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SILICA Microcontroller Solutions



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SPEAr[®] Embedded Processors

ARM[®]9 and Cortex[™]-A9 based MPU family:
Powerful Processing and Flexibility to serve a broad range of applications.



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SPEAr® – Embedded Microprocessor
SPEAr® Devices, based on ARM® Core Architecture,
offer Substantial Processing Power and Wide Peripheral Support 5

SPEAr1310 – Embedded Microprocessor
Dual ARM® Cortex™-A9 Cores Enable High-Performance,
High-connectivity and Industrial Applications..... 6

SPEAr1340 – Embedded Microprocessor
Dual ARM® Cortex™-A9 Core eMPU for User Interfaces/
Multimedia in Computing and Industrial Applications 8

SPEAr300
SPEAr® Embedded MPU with ARM926EJ-STC Core –
A Smart Choice for VoIP, HMI and Security Applications 10

SPEAr310
SPEAr® Embedded MPU with ARM926EJ-STC Core –
A Smart Choice for Telecom and Connectivity Applications 12

SPEAr320
SPEAr® Embedded MPU with ARM926EJ-STC Core –
A Smart Choice for Factory Automation and HMI oriented Applications 14

SPEAr600
SPEAr® Embedded MPU with Dual ARM926EJ-STC Core 16

SPEAr® Devices, based on ARM Core Architecture, offer Substantial Processing Power and Wide Peripheral Support

Embedded applications today demand increasingly higher levels of performance and power efficiency for computing, communication, control, security and multimedia. ST’s SPEAr® embedded MPUs meet these challenges head-on with state-of-the-art architecture, silicon technology and intellectual property, targeting networked devices used for communication, display and control of a broad range of applications.

The SPEAr family of embedded microprocessors are based on ARM cores: a single ARM926EJ-S core for the SPEAr300 series, dual ARM926EJ-S cores for the SPEAr600, and dual Cortex™-A9 cores for the SPEAr1300 series.

Key Features

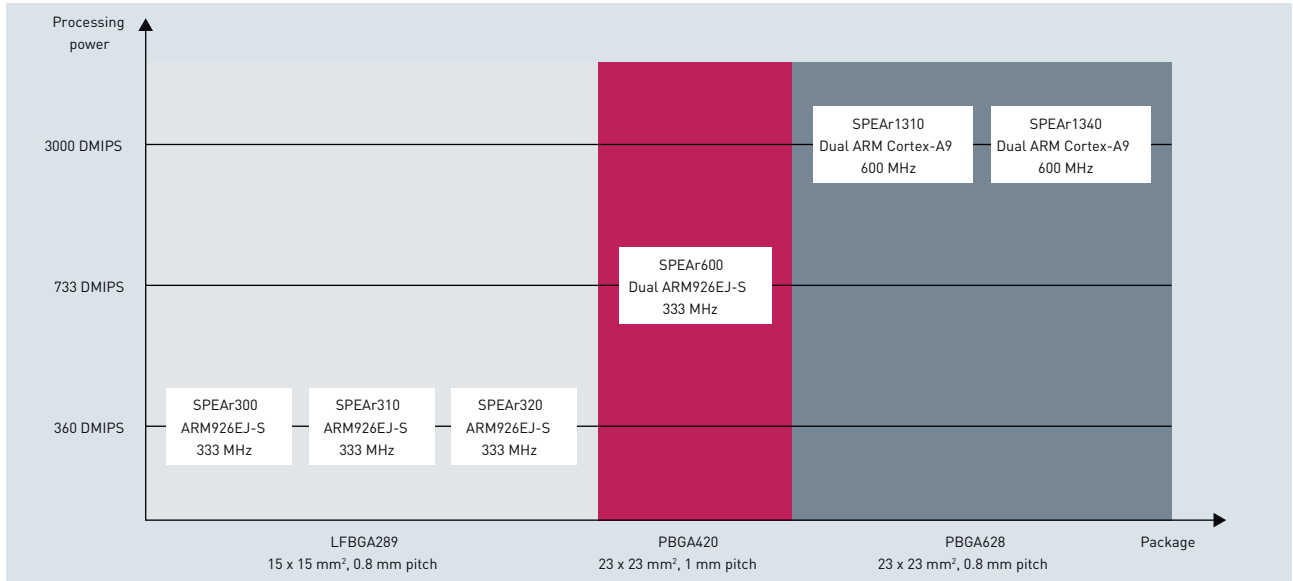
- The family presents a scalable processing power range, depending on the type and number of cores used

- Within a series, each device targets a specific application segment, and offers peripherals and controllers in line with this specialization
- All SPEAr embedded microprocessors embed the external memory management function via a dynamic memory controller

Key Benefits

- ST’s low-power technology makes SPEAr microprocessors extremely power-efficient, permitting portable applications to run longer without recharging, saving operating costs for end customers and allowing your applications to meet the most stringent regulatory standards
- Standard core architecture is supported by a wide range of 3rd party tool providers, for easy development

SPEAr Family of Embedded Microprocessors





Dual ARM® Cortex™-A9 Cores Enable High-Performance, Extended Connectivity for Industrial and Embedded Computer oriented Applications



ST’s SPEAr1310 is a part of the growing SPEAr family of embedded MPUs for networking. It offers an unprecedented combination of processing performance and extreme power reduction control for next-generation communication applications. The SPEAr1310 is based on ARM’s new multicore technology (Cortex-A9 SMP/AMP), and is manufactured using ST’s 55 nm HCMOS low-power silicon process.

Key Features

- CPU subsystem
 - Dual ARM Cortex-A9 cores, 600 MHz
 - Supports both symmetric (SMP) and asymmetric (AMP) multiprocessing
- 32 + 32-Kbyte L1 instruction/data cache per core with parity check
- Shared 512-Kbyte L2 cache (ECC protected)
- Accelerator coherence port
- Bus: 64-bit multilayer network-onchip
- Memories
 - 32 Kbyte boot ROM
 - 32 Kbyte internal SRAM
 - Multiport controller (MPMC) for external DDR2-800/DDR3-1066 with ECC

- Controller (FSMC) for external Flash and SRAM
- Controller (SMI) for external serial
- NOR Flash
- Controls external peripherals
 - TFT LCD display up to 1920 x 1080 (60 Hz)
 - Touchscreen I/F
 - 9 x 9 keyboard
 - Memory card interface
- Connectivity
 - Gigabit (with IEEE1588) and Fast Ethernet ports
 - 3x PCIe 2.0/SATA
 - 3x USB 2.0 (Host/OTG)
 - 2x CAN 2.0 a/b interfaces
 - 2x HDLC RS485
 - I²S, UART, I²C and SPI
- Expansion interface (EXPI)
- Security: C3 cryptographic accelerator
- Power saving
 - Power islands for leakage reduction
 - IP clock gating for dynamic power reduction
 - Dynamic frequency scaling
- Package: PBGA628 (23 x 23 mm², 0.8 mm pitch)

Overview

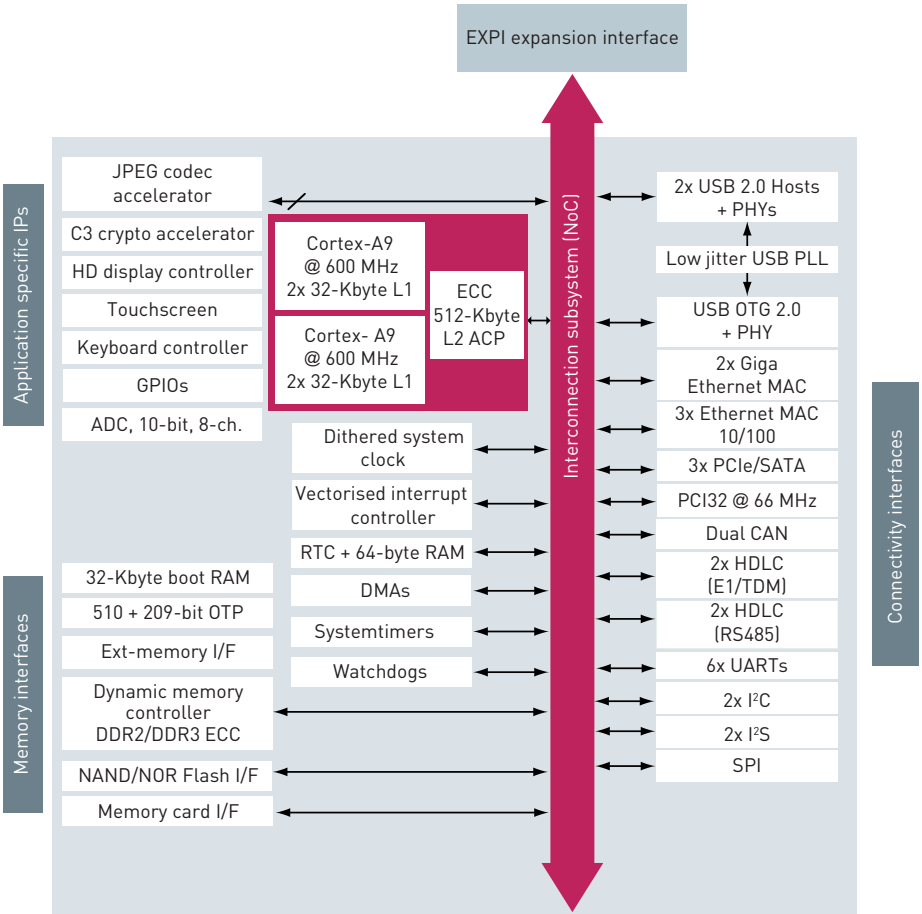
The SPEAr1310 combines two ARM Cortex-A9 cores with a DDR3 (third-generation, double-data-rate) memory interface. Together with ST’s low-power 55 nm HCMOS process technology, the SPEAr1310 delivers high computing power and customisability for a variety of embedded applications, with a high degree of cost competitiveness. The dual processors support both fully symmetric and asymmetric operations, at speeds of 600 MHz (industrial worst-case conditions) for an equivalent of 3000 DMIPS.

In addition to unrivalled low power and multiprocessing capabilities, this new eMPU offers the innovative network-on-chip (NoC) technology. NoC is a flexible communications architecture that enables multiple and different traffic profiles while maximising data throughput in the most performance and power-efficient way.

Equipped with an integrated DDR2/DDR3 memory controller and a full set of connectivity peripherals, including USB, SATA, PCIe (with integrated PHY) and Giga Ethernet MAC, the SPEAr1310 targets high-performance, embedded-

control applications across the communication, computer peripherals and industrial automation markets. Cache memory coherency with hardware accelerators and I/O blocks increases throughput and simplifies software development. The accelerator coherency port (ACP), together with the device’s NoC routing capabilities, addresses the latest application requirements for hardware acceleration and I/O performance. ECC (Error Correction Coding) protection against soft and hard errors on both DRAM and L2 cache memories significantly improves the mean-time-between-failures for enhanced reliability.

SPEAr1310 Block Diagram





Dual ARM® Cortex™ A9 Core eMPU for User Interfaces/Multimedia in Computing and Industrial Applications



ST’s SPEAr1340 is a part of the growing SPEAr family of embedded MPUs. Combining dual Cortex™-A9 cores with the ARM® Mali-200 GPU, it targets applications ranging from high-resolution video conferencing and security cameras, to webconnected devices. The SPEAr1340 is based on ARM’s new multi-core technology (Cortex™-A9 SMP/AMP), and manufactured with ST’s 55 nm HCMOS low-power silicon process.

Key Features

- CPU subsystem
 - Dual ARM® Cortex™-A9 cores, 600 MHz
 - Supports both symmetric (SMP) and asymmetric (AMP) multiprocessing
 - 32 + 32-Kbyte L1 cache per core
 - Shared 512 Kbyte L2 cache
 - Accelerator coherence port
- Bus: 64-bit multilayer NoC
- Memories
 - 32 Kbyte boot ROM
 - 32 Kbyte internal SRAM
 - Multiport controller (MPMC) formexternal DDR2-800/DDR3-1066
 - Controller (FSMC) for external Flash and SRAM
 - Controller (SMI) for external serial NOR Flash

- Connectivity
 - Giga/Fast Ethernet
 - 1x PCIe 2.0/SATA
 - 3x USB 2.0 (Host/OTG)
 - I²S, UART, and I²C
- Controls external peripherals
 - TFT LCD display up to 1920 x 1080 (60 Hz)
 - Touchscreen I/F
 - 9 x 9 keyboard
 - Memory card interface
- Multimedia
 - Mali-200 2D/3D GPU, up to 1080p, OpenGL ES 2.0, OpenVG 2.0
 - Multi-standard HD video decoder and encoder, up to 1080p
 - Digital video input port with alternate configuration for 4 camera interfaces
 - 7.1 multichannel surround audio
- Security: C3 cryptographic accelerator
- Power saving
 - Power islands for leakage reduction
 - IP clock gating for dynamic power reduction
 - Dynamic frequency scaling
- Package: PBGA628 [23 x 23 mm², 0.8 mm pitch]

Overview

ST’s SPEAr1340 integrates a powerful ARM Mali 200 graphics processing unit for advanced 2D and 3D acceleration for user interfaces, navigation, browsing and gaming. The new device also embeds a hardware video encoder and a decoder supporting major compression standards (including H.264 and AVS), with video resolution up to 1080p and 30 frames per second. These capabilities enable multiple concurrent video flows in applications like surveillance and video-conferencing.

Hardware implementations of graphic and video capabilities in the SPEAr1340 result in state-of-the art multimedia performance at ultra-low power consumption. Meanwhile, the two Cortex™-A9 cores are available to performing concurrent tasks as required. With its multiple interfaces, including I²S and S/PDIF, the SPEAr1340 also provides excellent audio capabilities, handling up to 7.1 surround-sound configurations in both input and output paths.

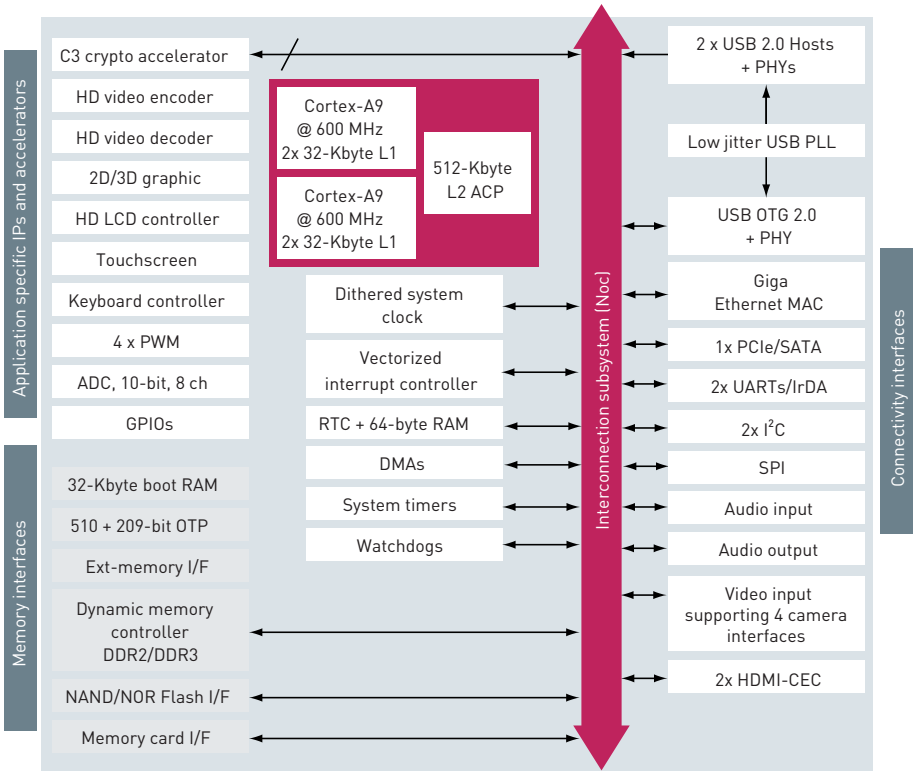
In security, the SPEAr1340 integrates a multi-standard cryptographic engine and One-Time Programmable (OTP) registers for unique identification and external flash memory anti-tamper protection.

Manufactured in ST’s low-power 55 nm HCMOS (high-speed CMOS) process technology, this new microprocessor benefits from the state-of-the-art SPEAr1300 architecture, which combines the unrivalled low-power and multi-processing capabilities of two ARM Cortex™-A9 cores with innovative Network-on-Chip (NoC) technology.

Design support

Information on development tools and evaluation boards, as well as downloads of the latest STLinux OS, firmware, and technical documentation, can be found on: www.st.com/spear

SPEAr1340 Block Diagram





SPEAr® Embedded MPU with ARM926EJ-STM Core – A Smart Choice for VoIP, HMI and Security Applications



Highly integrated, the SPEAr300 is a 32-bit ARM926EJ-S -based eMPU for cost-sensitive applications requiring significant processing and connectivity capabilities at lower power consumption.

The SPEAr300 delivers everything you want for an IP phone, human-machine interface, and security applications. However, this versatile device is also perfectly suited to many other embedded applications.

Learn more about this and other SPEAr® products, development kits, reference designs and our regional design-in support centers by visiting www.st.com/spear.

Key Features

- ARM926EJ-S core runs up to 333 MHz
- High-performance 8-channel DMA
- Dynamic power-saving features
- Memory:
 - 32-Kbyte ROM and up to 57-Kbyte internal SRAM
 - LPDDR-333/DDR2-666 interface
 - Serial SPI Flash interface
 - Flexible static memory controller (FSMC) up to 16-bit data bus width, supporting external SRAM, NAND/NOR Flash memories, peripherals and FPGAs
 - SDIO/MMC card interface
- Security:
 - Cryptographic accelerator (DES/3DES/AES/SHA1)
- Connectivity:
 - USB 2.0 (2 hosts, 1 device)
 - Fast Ethernet (MII port)
 - SPI, I²C, I²S, UART and fast IrDA interfaces
 - Up to 8 I²C/SPI chip selects
 - TDM bus (512 timeslots)

- Peripherals supported:
 - Camera interface (ITU-601/656 and CSI2 support)
 - LCD controller (resolutions up to 1024 x 768 and up to 24 bpp)
 - Touchscreen support
 - 9 x 9 keyboard controller
 - Glueless management of up to 8 SLICs/codecs
- Miscellaneous functions:
 - Integrated real-time clock, watchdog, and system controller
 - 8-channel 10-bit ADC, 1 MSPS
 - 1-bit DAC
 - JPEG codec accelerator
 - 6 general-purpose 16-bit timers with capture mode and programmable prescaler
 - Up to 44 GPIOs with interrupt capability
- Package: LFBGA289 (15 x 15 mm², pitch 0.8 mm)

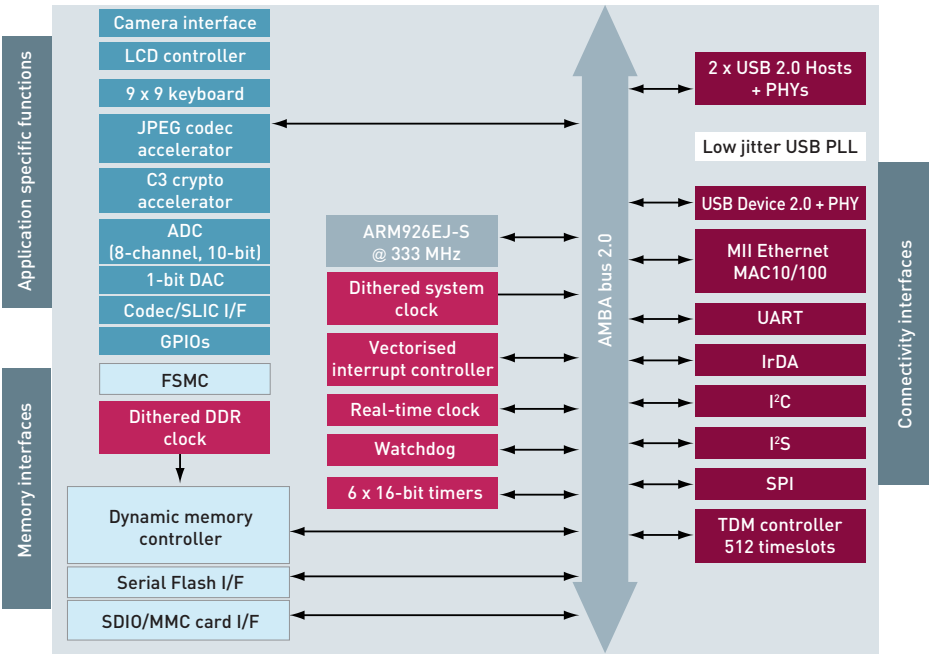
SPEAr®: Flexible, powerful eMPUs with high connectivity

Embedded applications today demand increasingly higher levels of performance and power efficiency for computing, communication, control, security and multimedia. ST's SPEAr® family of embedded MPUs meet these challenges head-on with state-of-the-art architecture, silicon technology and intellectual property, targeting networked devices used for communication, display and control.

The new SPEAr300 delivers robust processing with a 333 MHz ARM926EJ-S core that supports complex operating systems like Linux, sophisticated user interfaces and microbrowsers. The CPU also offers 16 Kbytes of data cache, 16 Kbytes of instruction cache, JTAG and ETM (embedded trace macrocell) for debug operations.

A set of tailored peripheral interfaces, hardware accelerators and controllers make the SPEAr300 a smart choice for HMI, security and IP phone applications.

SPEAr300 Block Diagram





SPEAr® Embedded MPU with ARM926EJ-STM Core –
A Smart Choice for Telecom and Connectivity Applications



Highly integrated, the SPEAr310 is a 32-bit ARM926EJ-S -based eMPU for cost-sensitive applications requiring significant processing and connectivity capabilities at lower power consumption.

The SPEAr310 delivers everything you want for telecom applications. However, this versatile device is also perfectly suited to many other embedded applications. Learn more about this and other SPEAr® products, development kits, reference designs and our regional design-in support centers by visiting www.st.com/spear.

Key Features

- ARM926EJ-S core runs up to 333 MHz
- High-performance 8-channel DMA
- Dynamic power-saving features
- Memory:
 - 32-Kbyte ROM and up to 8-Kbyte internal SRAM
 - LPDDR-333/DDR2-666 interface
 - Serial SPI Flash interface
 - Flexible static memory controller (FSMC), up to 32-bit data bus width, supporting external SRAM, NAND/NOR Flash memories, peripherals and FPGAs
- Connectivity:
 - USB 2.0 (2 hosts, 1 device)
 - 1 fast Ethernet MII port
 - 4 fast Ethernet SMII ports
 - SPI, I²C and fast IrDA interfaces
 - 6 UART interfaces
 - TDM bus (128 timeslots with 64 HDLC channels)
 - 2 HDLC ports with RS485 support
- Security:
 - Cryptographic accelerator (DES/3DES/AES/SHA1)
- Miscellaneous functions:
 - Integrated real-time clock, watchdog, and system controller

- 8-channel 10-bit ADC, 1 MSPS
- JPEG codec accelerator
- 6 general-purpose 16-bit timers with capture mode and programmable prescaler
- Up to 102 GPIOs with interrupt capability
- Package: LFBGA289 (15 x 15 mm², pitch 0.8 mm)

SPEAr®: Flexible, powerful eMPUs with high connectivity
Embedded applications today demand increasingly higher levels of performance and power efficiency for computing, communication, control, security and multimedia.

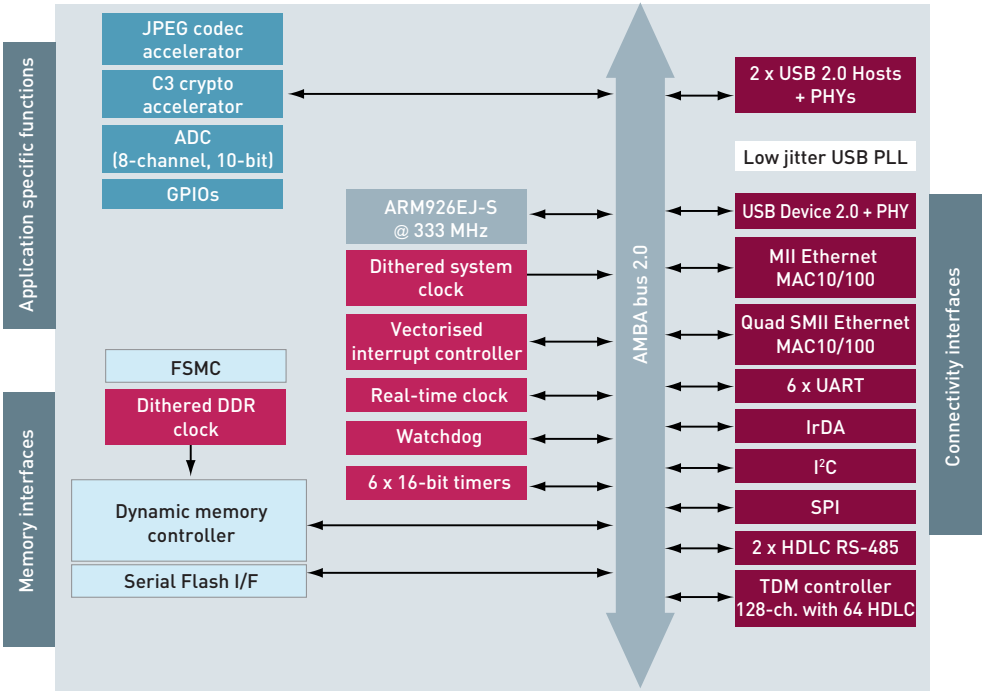
ST’s SPEAr® family of embedded MPUs meet these challenges head-on with state-of-the-art architecture,

silicon technology and intellectual property, targeting networked devices used for communication, display and control.

The new SPEAr310 delivers robust processing with a 333 MHz ARM926EJ-S core that supports complex operating systems like Linux, sophisticated user interfaces and microbrowsers. The CPU also offers 16 Kbytes of data cache, 16 Kbytes of instruction cache, JTAG and ETM (Embedded Trace Macrocell) for debug operations.

A set of tailored peripheral interfaces, hardware accelerators and controllers make the SPEAr310 a smart choice for telecom and connectivity applications.

SPEAr310 Block Diagram





SPEAr® Embedded MPU with ARM926EJ-STM Core – A Smart Choice for Factory Automation and HMI oriented Applications



Highly integrated, the SPEAr320 is a 32-bit ARM926EJ-S -based eMPU for cost-sensitive applications requiring significant processing and connectivity capabilities at lower power consumption.

The SPEAr320 delivers everything you want for factory automation and consumer applications. However, this versatile device is also perfectly suited to many other embedded applications. Learn more about this and other SPEAr® products, development kits, reference designs and our regional design-in support centers by visiting www.st.com/spear.

Key Features

- ARM926EJ-S core runs up to 333 MHz
- High-performance 8-channel DMA
- Dynamic power-saving features
- Memory:
 - 32-Kbyte ROM and up to 8-Kbyte internal SRAM
 - LPDDR-333/DDR2-666 interface
 - SDIO/MMC card interface
 - Serial SPI Flash interface
 - Flexible static memory controller (FSMC), up to 16-bit data bus width, supporting external SRAM, NAND/NOR Flash memories, peripherals and FPGAs
- Security:
 - Cryptographic accelerator (DES/3DES/AES/SHA1)
- Connectivity:
 - USB 2.0 (2 hosts, 1 device)
 - 2 fast Ethernet ports (MII/SMII ports)
 - 2 CAN interfaces
 - I²S and fast IrDA interfaces
 - 3 SPI ports
 - 2 I²C interfaces
 - 3 UART interfaces
 - 1 standard parallel device port

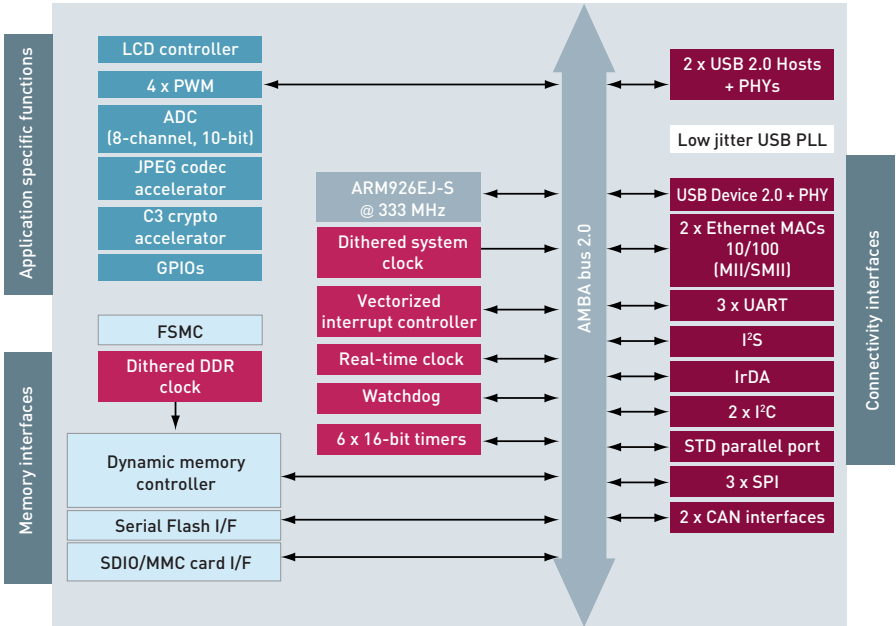
- Peripherals supported:
 - LCD controller (resolutions up to 1024 x 768 and up to 24 bpp)
 - Touchscreen support
- Miscellaneous functions:
 - Integrated real time clock, watchdog and system controller
 - 8-channel 10-bit ADC, 1 MSPS
 - 4 PWM timers
 - JPEG codec accelerator
 - 6 general-purpose 16-bit timers with capture mode and programmable prescaler
 - Up to 102 GPIOs with interrupt capability
- Package: LFBGA289 (15 x 15 mm², pitch 0.8 mm)

SPEAr®: Flexible, powerful eMPUs with high connectivity

Embedded applications today demand increasingly higher levels of performance and power efficiency for computing, communication, control, security and multimedia. ST's SPEAr® family of embedded MPUs meet these challenges head-on with state-of-the-art architecture, silicon technology and intellectual property, targeting networked devices used for communication, display and control.

The new SPEAr320 delivers robust processing with a 333 MHz ARM926EJ-S core that supports complex operating systems like Linux, sophisticated user interfaces and microbrowsers. The CPU also offers 16 Kbytes of data cache, 16 Kbytes of instruction cache, JTAG and ETM (embedded trace macrocell) for debug operations. A set of tailored peripheral interfaces, hardware accelerators and controllers make the SPEAr320 a smart choice for factory automation and HMI oriented applications.

SPEAr320 Block Diagram





SPEAr® Embedded MPU with Dual ARM926EJ-STM Core



The SPEAr600 is a highly integrated eMPU with flexible memory support, powerful connectivity features and programmable LCD interface.

High-performance dual 32-bit ARM926EJ-S CPU cores make this part the right choice for cost-sensitive applications that require extra computational power. The SPEAr600 is a versatile device which supports a wide range of embedded applications.

Learn more about this and other SPEAr® products, development kits, reference designs and our regional design-in support centers by visiting www.st.com/spear.

Key Features

- Dual ARM926EJ-S cores run up to 333 MHz
- High-performance 8-channel DMA
- Dynamic power-saving features
- Up to 733 DMIPS
- Memory:
 - 32 Kbytes ROM and up to 8 Kbytes internal SRAM
 - External DRAM interface: 8/16-bit DDR1-400/DDR2-666
 - Flexible Static Memory Controller (FSMC) supporting parallel NAND Flash memory interface
 - Serial NOR Flash memory interface
- Connectivity:
 - USB 2.0 (2 hosts, 1 device)
 - 1 Giga Ethernet (GMII port)
 - I²C and fast IrDA interfaces
 - 3 SPI ports
 - 3 I²S interfaces (1 stereo input, 2 stereo outputs)
 - 2 UART interfaces
- Peripherals supported:
 - LCD controller (resolutions up to 1024 x 768 and up to 24 bpp)
 - Touchscreen support

- Miscellaneous functions:
 - Integrated real time clock, watchdog, and system controller
 - 8-channel 10-bit ADC, 1 MSPS
 - JPEG codec accelerator
 - 10 general-purpose 16-bit timers with capture mode and programmable prescalers
 - 10 GPIO bidirectional signals with interrupt capabilities
 - External 32-bit local bus
- Package: PBGA420 (23 x 23 mm², pitch 1 mm)

SPEAr®: Flexible, powerful eMPUs with high connectivity

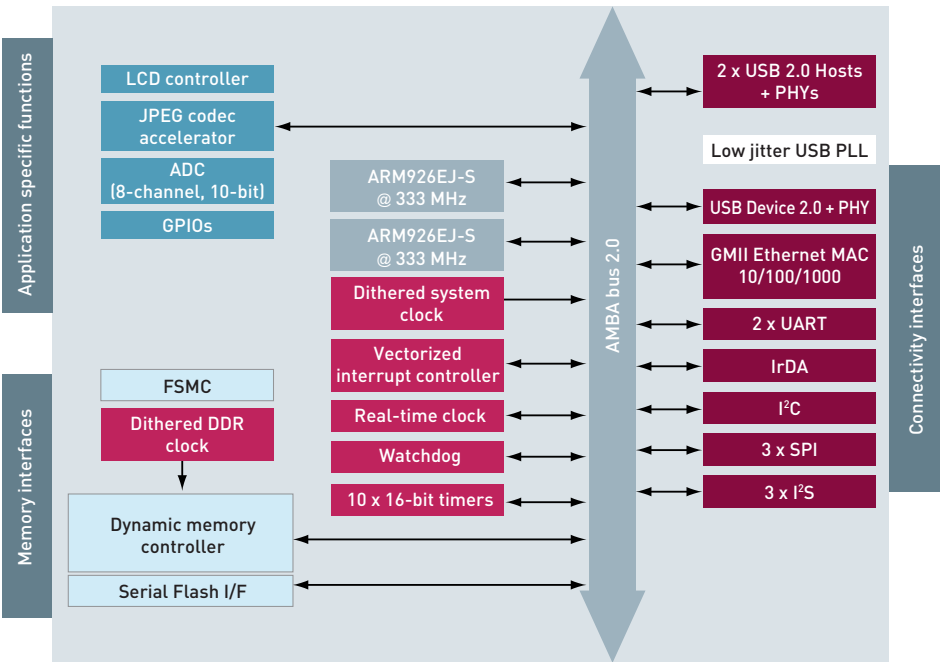
Embedded applications today demand increasingly higher levels of performance and power efficiency for computing, communication, control, security and multimedia.

ST's SPEAr® family of embedded MPUs meet these challenges head-on with state-of-the-art architecture, silicon technology and intellectual property, targeting networked devices used for communication, display and control.

The new SPEAr600 offers dual 333 MHz ARM926EJ-S cores that can support robust general-purpose processing and dedicated real-time processing together. The device supports complex operating systems like Linux, sophisticated user interfaces and microbrowsers. Both processors offer 16 Kbytes of data cache, 16 Kbytes of instruction cache, JTAG and ETM (embedded trace macrocell) for debug operations.

Furthermore, the SPEAr600 offers unique flexibility by externalising its local bus so that external peripherals can be added.

SPEAr600 Block Diagram





Think Microcontroller. Think **Silica**.

You know the big
microcontroller
design problem?

Distributors propose
you a core...



...or sometimes a
few more
(if you're lucky).



Or they sell you
the old stuff!



Hardware, Software,
Tools – you get
everything in bits
and pieces...



...and you are left
alone in fitting
all together.



How about
the idea
of having
a partner
who handles
everything?



Think of your next
microcontroller design.



 **SILICA**
An Avnet Company

SILICA Offices

AUSTRIA

Avnet EMG Elektronische Bauelemente GmbH
 Schönbrunner Str. 297 - 307 • A-1120 Wien
 Phone: +43 1 86642-300 • Fax: +43 1 86642-350
 wien@silica.com

BELGIUM

Avnet Europe Comm. VA
 Eagle Building • Kouterveldstraat 20B
 B-1831 Diegem
 Phone: +32 2 709 90 00 • Fax: +32 2 709 98 10
 diegem@silica.com

CZECH REPUBLIC (SLOVAKIA)

Avnet
 Argentinská 38/286 • CZ-170 00 Praha 7
 Phone: +420 2 34091031 • Fax: +420 2 34091030
 praha@silica.com

DENMARK

Avnet Nortec A/S
 Ellekær 9 • DK-2730 Herlev
 Phone: +45 43 22 80 10 • Fax: +45 43 22 80 11
 herlev@silica.com

FINLAND (ESTONIA)

Avnet Nortec Oy
 Pihatörmä 1B • FIN-02240 Espoo
 Phone: +358 20 749 9200 • Fax: +358 20 749 9280
 helsinki@silica.com

FRANCE (TUNISIA)

Avnet EMG France SA
 Immeuble Carnot Plaza • 14 Avenue Carnot
 F-91349 Massy Cedex
 Phone: +33 1 64 47 29 29 • Fax: +33 1 64 47 00 84
 paris@silica.com

Avnet EMG France SA
 Parc Club du Moulin à Vent • Bât 40
 33, rue du Dr. G. Lévy • F-69693 Vénissieux Cedex
 Phone: +33 4 78 77 13 60 • Fax: +33 4 78 77 13 99
 lyon@silica.com

Avnet EMG France SA
 Les Peupliers II • 35, avenue des Peupliers
 F-35510 Cesson Sévigné
 Phone: +33 2 99 83 84 85 • Fax: +33 2 99 83 80 83
 rennes@silica.com

Avnet EMG France SA
 Parc de la Plaine 35 • avenue Marcel Dassault –
 BP 5867 • F-31506 Toulouse Cedex 5
 Phone: +33 5 62 47 47 60 • Fax: +33 5 62 47 47 61
 toulouse@silica.com

GERMANY

Avnet EMG GmbH
 Gruber Str. 60 C • D-85586 Poing
 Phone: +49 8121 777 02 • Fax: +49 8121 777 531
 muenchen@silica.com

Avnet EMG GmbH
 Rudower Chaussee 12 a • D-12489 Berlin
 Phone: +49 30 214882-0 • Fax: +49 30 214882-33
 berlin@silica.com

Avnet EMG GmbH
 Berliner Platz 9 • D-44623 Herne
 Phone: +49 2323 96466-0 • Fax: +49 2323 96466-60
 herne@silica.com

Avnet EMG GmbH
 Wolfenbütteler Str. 22 • D-38102 Braunschweig
 Phone: +49 531 22073-0 • Fax: +49 531 2207335
 braunschweig@silica.com

Avnet EMG GmbH
 Gutenbergstraße 15 • D-70771 Leinfelden-Echterdingen
 Phone: +49 711 78260-01 • Fax: +49 711 78260-200
 stuttgart@silica.com

Avnet EMG GmbH
 Carl-Zeiss-Str. 14 - 18 • D-65520 Bad Camberg
 Phone: +49 6434 9046 30 • Fax: +49 6434 90 46 33
 badcamberg@silica.com

HUNGARY

Avnet
 Budafoki út 91-93 • IP WEST/Building B
 H-1117 Budapest
 Phone: +36 1 43 67215 • Fax: +36 1 43 67213
 budapest@silica.com

ITALY

Avnet EMG Italy S.r.l.
 Via Manzoni 44, I-20095 Cusano Milanino MI
 Phone: +39 02 660 921 • Fax: +39 02 66092 333
 milano@silica.com

Avnet EMG Italy S.r.l.
 Viale dell' Industria, 23 • I-35129 Padova (PD)
 Phone: +39 049 8073689 • Fax: +39 049 773464
 padova@silica.com

Avnet EMG Italy S.r.l.
 Via Panciatichi, 40 • I-50127 Firenze (FI)
 Phone: +39 055 4360392 • Fax: +39 055 431035
 firenze@silica.com

Avnet EMG Italy S.r.l.
 Via Scaglia Est, 144 • I-41100 Modena (MO)
 Phone: +39 059 351300 • Fax: +39 059 344993
 modena@silica.com

Avnet EMG Italy S.r.l.
 Via Zoe Fontana, 220 • I-00131 Roma Tecnocittà
 Phone: +39 06 4131151 • Fax: +39 06 4131161
 roma@silica.com

Avnet EMG Italy S.r.l.
 Corso Susa, 242 • I-10098 Rivoli (TO)
 Phone: +39 011 204437 • Fax: +39 011 2428699
 torino@silica.com

NETHERLANDS

Avnet B.V.
 Takkebijsters 2 • NL-4817 BL Breda
 Phone: +31 (0)76 57 22 700 • Fax: +31 (0)76 57 22 707
 breda@silica.com

NORWAY

Avnet Nortec AS
 Hagaløkkveien 7 • Postboks 63 • N-1371 Asker
 Phone: +47 6677 3600 • Fax: +47 6677 3677
 asker@silica.com

POLAND (LATVIA/LITHUANIA)

Avnet EM Sp. z o.o.
 Street Marynarska 11 • PL-02-674 Warszawa
 (Building Antares, 5th Floor)
 Phone: +48 22 25 65 760 • Fax: +48 22 25 65 766
 warszawa@silica.com

PORTUGAL

Avnet Iberia S.A.
 Tower Plaza • Rot. Eng. Edgar Cardoso, 23
 Piso 14 • Sala E
 P-4400-676 Vila Nova de Gaia
 Phone: +35 1 223 779 502 • Fax: +35 1 223 779 503
 porto@silica.com

RUSSIA (BELARUS, UKRAINE)

Avnet
 Korovinskoye Chaussee 10 • Building 2
 Office 25 • RUS-127486 Moscow
 Phone: +7 495 9371268 • Fax: +7 495 9372166
 moscow@silica.com

Avnet
 Polustrovsky Prospect, 43, of.422
 RUS-195197 Saint Petersburg
 Phone: +7 (812) 635 81 11 • Fax: +7 (812) 635 81 12
 stpetersburg@silica.com

SLOVENIA (BULGARIA, CROATIA, BOSNIA, MACEDONIA, SERBIA/MONTENEGRO, ROMANIA)

Avnet
 Dunajska c. 159 • SLO-1000 Ljubljana
 Phone: +386 (0)1 560 9750 • Fax: +386 (0)1 560 9878
 ljubljana@silica.com

SPAIN

Avnet Iberia S.A.
 C/Chile,10 • plta. 2ª, ofic 229 • Edificio Madrid 92
 E-28290 Las Matas (Madrid)
 Phone: +34 91 372 71 00 • Fax: +34 91 636 97 88
 madrid@silica.com

Avnet Iberia S.A.
 C/Mallorca, 1 al 23 • 2ª plta.1A • E-08014 Barcelona
 Phone: +34 93 327 85 30 • Fax: +34 93 425 05 44
 barcelona@silica.com

Avnet Iberia S.A.
 Plaza Zabalgane, 12 • Bajo Izqda.
 E-48960 Galdácano (Vizcaya)
 Phone: +34 944 57 27 77 • Fax: +34 944 56 88 55
 bilbao@silica.com

SWEDEN

Avnet Nortec AB
 Esplanaden 3D • BOX 1830 • S-17127 Solna
 Phone: +46 8 587 461 00 • Fax: +46 8 587 461 01
 stockholm@silica.com

SWITZERLAND

Avnet EMG AG
 Gaswerkstr. 32 • CH-4900 Langenthal
 Phone: +41 62 919 55 55 • Fax: +41 62 919 55 00
 langenthal@silica.com

TURKEY (GREECE, EGYPT)

Avnet
 Bayar Cad. Gülbahar Sok. Nr. 17/111-112
 TR- 34742 Kozytagi/Istanbul
 Phone: +90 216 361 89 58 • Fax: +90 216 361 89 27
 istanbul@silica.com

UNITED KINGDOM (IRELAND)

Avnet EMG Ltd.
 Avnet House • Rutherford Close
 Meadowway Stevenage, Herts • SG1 2EF
 Phone: +44 (0)1438 788310 • Fax: +44 (0)1438 788262
 stevenage@silica.com

Avnet EMG Ltd.
 Unit A5, 5 Ashworth House • Deakins Business Park
 The Hall Coppice • Egerton, Bolton • BL7 9RP
 Phone: +44 (0)1204 590270 • Fax: +44 (0)1204 590299
 bolton@avnet.eu

Avnet EMG Ltd.
 Cherrycourt Way • Leighton Buzzard
 Bedfordshire • LU7 4YY
 Phone: +44 (0)1525 858204 • Fax: +44 (0)1525 858280
 leightonbuzzard@avnet.eu

Avnet EMG Ltd.
 Unit 5B • Waltham Park • White Waltham
 Berkshire • SL6 3TN
 Phone: +44 (0)1628 512912 • Fax: +44 (0)1628 512999
 maidenhead@avnet.eu

Avnet EMG Ltd.
 Chancery House • 1 Premier Way
 Abbey Park, Romsey • SO51 9AQ Southampton
 Phone: +44 (0)2380 263516 • Fax: +44 (0)2380 263514
 eastleigh@avnet.eu