

CROSSVOLT™

Low-Voltage Logic Selection Guide



3.3V



2.5V



1.8V



Fairchild Low-Voltage Logic Families

CROSSVOLT Low-Voltage Logic: Easy to Choose and Easy to Use

Easy to Choose

Fairchild Semiconductor developed the *CROSSVOLT* Logic Series to deliver a comprehensive product portfolio with solutions for every low-voltage design need. Fairchild's low-voltage family offerings include VCX™, LCX, LVT, LVX, Dual Supply Translators and TinyLogic™ devices to provide optimal solutions across the widest variety of applications. *CROSSVOLT* delivers maximum design flexibility, shortens time to market, and comes with all the selection tools you need to define the right product quickly.

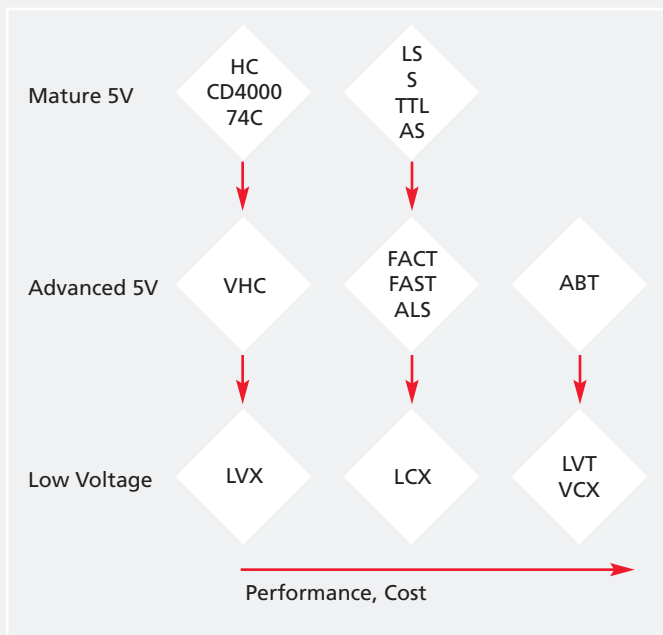
Easy to Use

Select the right *CROSSVOLT* device for your application today, and you can be confident that as supply voltages continue to drop *CROSSVOLT* will ensure fast, safe and easy migration into new designs without having to select new logic families.

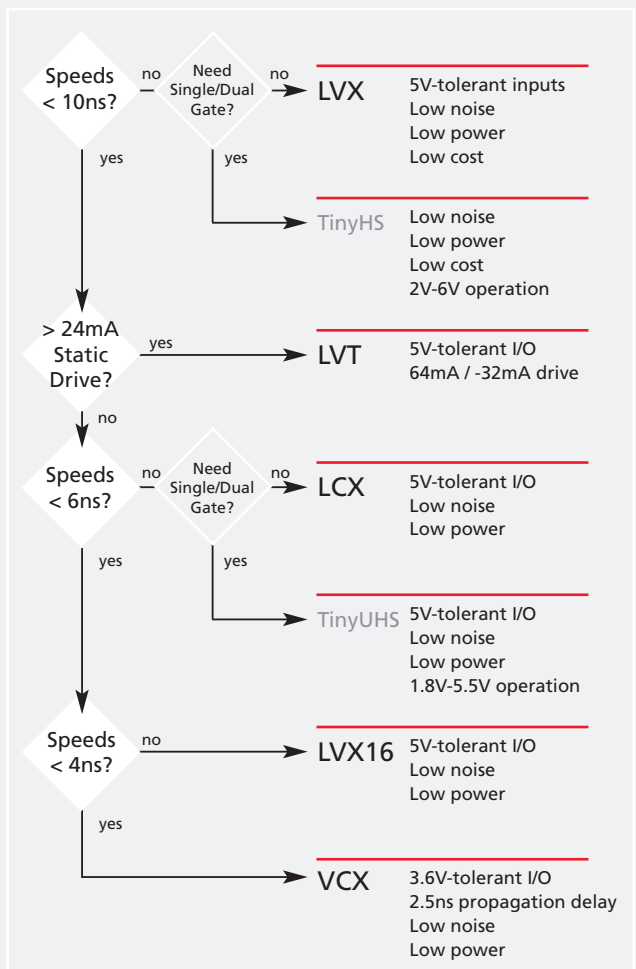
To use the *CROSSVOLT* Low-Voltage Selection Guide, select the performance attribute that is most important to your design—speed, dynamic power, capacitive derating, noise, etc.—and note the comparative family data. Then fine-tune your selection with the other criteria provided.

For additional literature and technical information on a specific product or family, call your local Fairchild Sales Office or visit us on line at: www.fairchildsemi.com/logic/lowvolt

Logic Migration and Low-Voltage Transition



Low-Voltage Decision Tree



CROSSVOLT™ Product Portfolio and Description

Buffers / Line Drivers
 Transceivers
 Registers / Flip-Flops
 Latches
 Counters
 Multiplexers
 Decoders / Demultiplexers
 Gates
 Dual Supply Translators
 26Ω Series Resistor
 Bushhold Options
 16 / 18 / 32 bit Functions
 8 / 10 / 12 bit Functions

CMOS										
VCX	●	●	●	●				●	●	High-speed CMOS enables interoperability between 3.3V and 2.5V systems, with 3.6V-tolerant inputs and outputs.
LCX	●	●	●	●	●	●	●	●	●	Offers 5V-tolerant inputs and outputs. Ideal for 3.3V applications requiring balanced drive capability, high speed, and low noise.
LVX	●	●	●	●	●	●	●	●	●	Offers 5V input tolerance that allows 5V CMOS to interface with 3.3V systems. Includes specialized dual-voltage translators.
BiCMOS										
LVT	●	●	●	●				●	●	High-speed, high-drive logic for 3.3V applications.
TinyLogic	●		●	●				●		Low-voltage, smallest footprint board space solutions in single- and dual-function logic.

Family Specification Comparison

	Specified Power Supply	Compatibility		Input Current †	Drive ††	Supply Current †	Speed †	
	V _{CC} ± 10%	V _L / V _H	V _{OL} / V _{OH}	I _L / I _H	I _{OL} / I _{OH}	I _{CC}	T _{PD}	
CMOS								
VCX (16bit) [◇]	3.3V / 2.5 / 1.8	TTL, CMOS	TTL, CMOS	-5μA / 5μA	24mA / -24mA	20μA	2.5 / 3.2ns	‡ input levels recognized by the device
LCX (8bit)	3.3V / 2.5	TTL, CMOS	TTL, CMOS	-5μA / 5μA	24mA / -24mA	10μA	6.5ns	‡‡ input levels the device is capable of driving
LCX (16bit)	3.3V / 2.5	TTL, CMOS	TTL, CMOS	-5μA / 5μA	24mA / -24mA	20μA	4.5ns	† maximum specification at maximum specified V _{CC}
LVX (8bit)	3.3V	TTL, CMOS	TTL, CMOS	-1μA / 1μA	4mA / -4mA	40μA	12.0ns	†† at maximum specified V _{CC}
BiCMOS								
LVT (8bit)	3.3V	TTL, CMOS	TTL, CMOS	-5μA / 1μA	64mA / -32mA	5mA	3.5ns	
LVT (16bit)	3.3V	TTL, CMOS	TTL, CMOS	-5μA / 1μA	64mA / -32mA	5mA	3.5ns	◇ C _{LOAD} =30pF
TinyHS**	2.0/3.0/4.5/6V *	CMOS	TTL, CMOS	-1μA / 1μA	2.6mA / -2.6mA	10μA	21ns	* not ±10%
TinyUHS**	1.8/2.5/3.3/5.5V	CMOS	TTL, CMOS	-10μA / 10μA	32mA / -32mA	20μA	4.5ns	** NAND Gate

Over-Voltage Tolerance

Over-voltage tolerance (OVT) allows a semiconductor device to accommodate input and output voltages that are higher than its operating voltage with no damage to the device or to signal integrity.

OVT is especially important in mixed-voltage design environments. OVT enables you to combine the features and benefits of devices with different performance attributes for more versatile and valuable system performance characteristics.

Over-Voltage Specifications

	I _I	I _{OFF}	I _{OZ}
CMOS			
VCX	5μA	10μA	10μA
LCX	5μA	10μA	5μA
LVX*	1μA	—	2.5μA
BiCMOS			
LVT	10μA	100μA	5μA

* 244 function

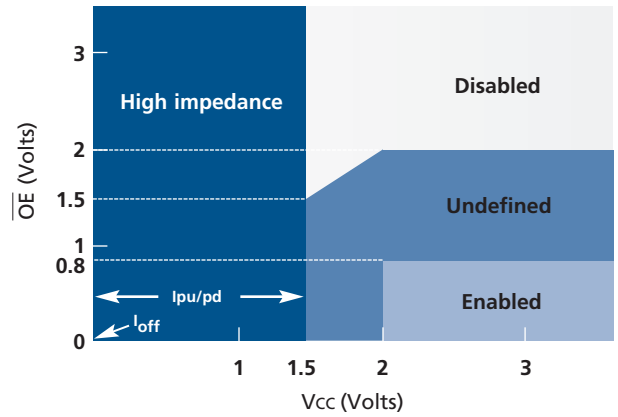
Note: All values pertain to '16244 function except LVX, which is a '244 function.

Power-Up / Power-Down

The power-up/power-down state diagram defines the stages that a device steps through when ramping up or ramping down V_{CC} . Each area represents a state that is controlled by internal power up/down gate sequencing, or by the Output Enable (\overline{OE}) pin.

High impedance—the initial state during power up—represents the conditions of device outputs due to internal gate sequencing. Generally, a high impedance state is maintained up to a V_T threshold for CMOS devices ($\sim 0.8V$), or up to two times V_{BE} for bipolar or BiCMOS devices ($\sim 1.5V$). This state can also be represented by the I_{OFF} and $I_{PU/PD}$ specifications.

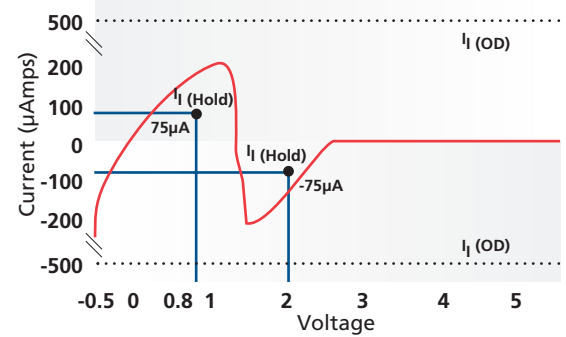
LVT products guarantee high impedance during power-up and power-down, allowing hot insertion capability.



Bushold

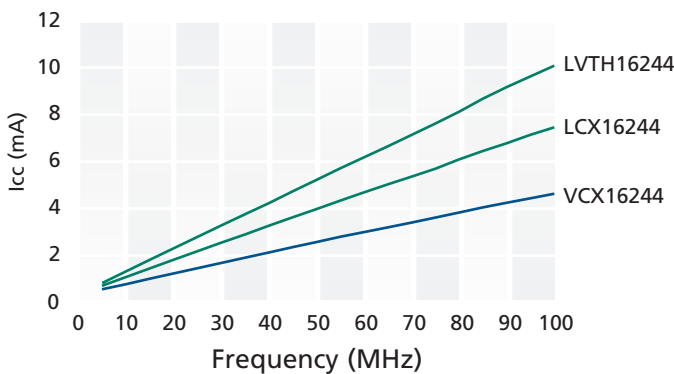
Devices featuring bushold will 'hold' the last known valid state of the input whenever a bus starts to float. This feature eliminates the need for external pullup or pulldown resistors. Devices with bushold may save space on a printed circuit board area and reduce cost.

Fairchild Semiconductor provides two types of bushold specifications. $I_{I(HOLD)}$ is the bushold input minimum drive and is specified at $\pm 75\mu A$. This is the minimum amount of current the circuit is capable of supplying. $I_{I(OD)}$ is the bushold input over-drive current to change state and is specified at $\pm 500\mu A$. This is the minimum amount of current that is necessary to overcome the bushold circuit, and cause the input to change states.



16 bit Dynamic Power

(typical process comparison, multiple outputs switching)



All figures represent typical performance values.

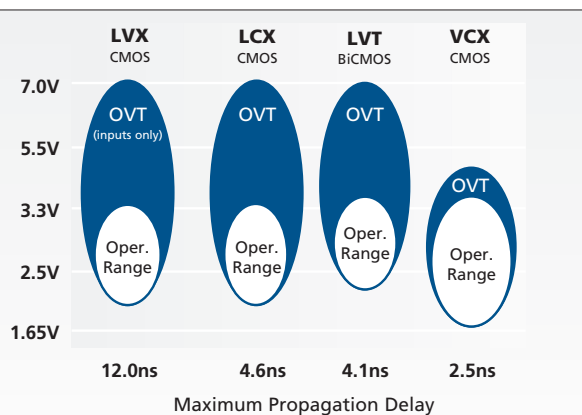
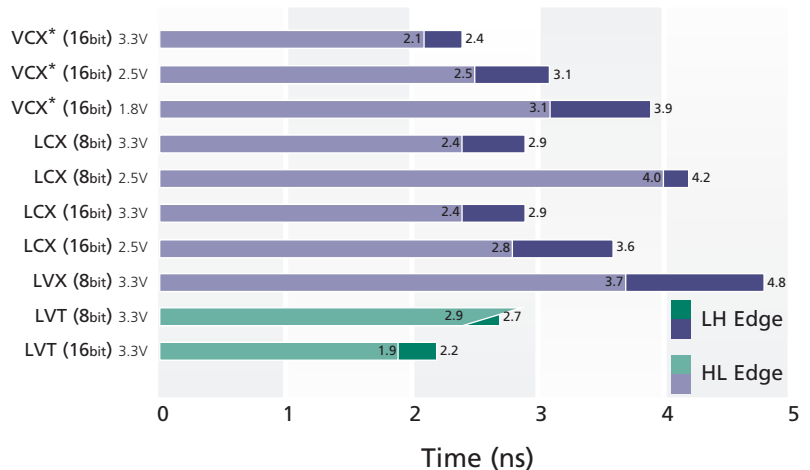
Dynamic Power (mA)

	5MHz	10MHz	35MHz	70MHz	90MHz
CMOS					
VCX (16bit)	0.23	0.46	1.61	3.15	4.02
LCX (16bit)	0.38	0.76	2.62	5.16	6.62
LCX (8bit)	0.36	0.72	2.47	4.92	6.18
LVX (8bit)	0.18	0.38	1.36	2.63	3.02
BiCMOS					
LVT (16bit)	0.50	1.01	3.52	6.99	9.08
LVT (8bit)	0.50	1.51	6.98	14.93	19.89

Single output switching @ 0pF, C_{LOAD}
All figures represent typical performance values.
 $V_{CC}=3.3V$

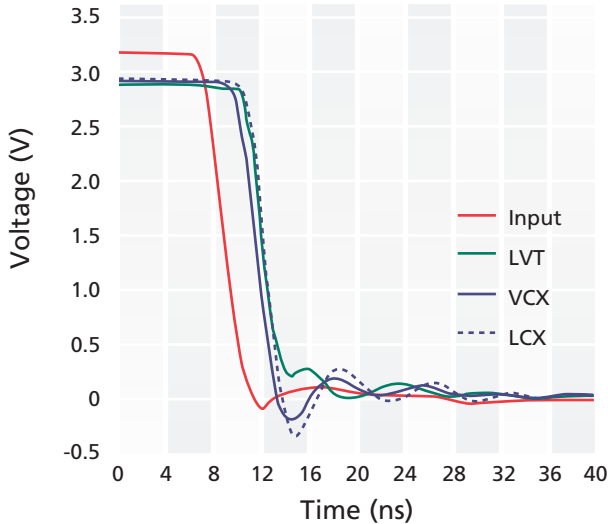
Output Rise and Fall Time

$C_{LOAD}=50pF$,
* $C_{LOAD}=30pF$



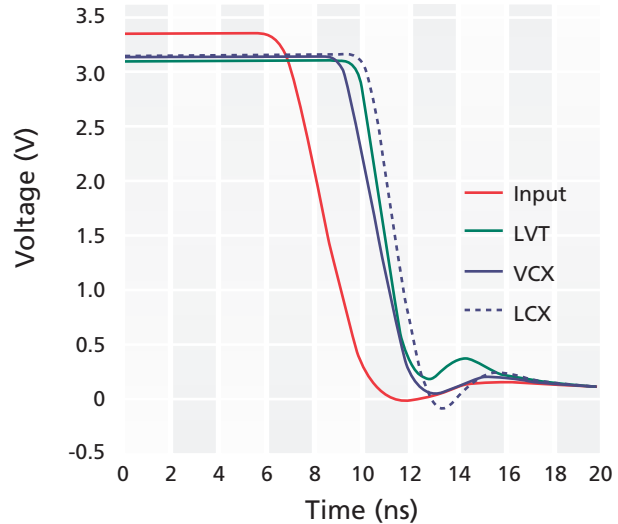
Note: All values pertain to '16244 function except LVX, which is a '244 function.

Active Edge Rate High-to-Low Multiple Outputs Switching*



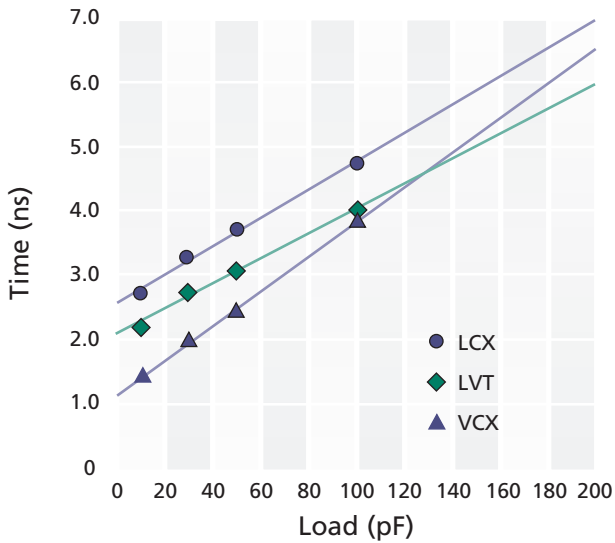
*16244 function, V_{CC}=3.3V

Active Edge Rate High-to-Low Single Output Switching*



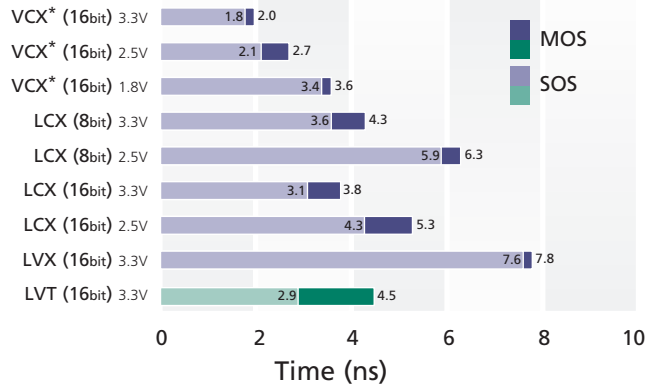
*16244 function, V_{CC}=3.3V

Capacitive Derating*



*16244 function, V_{CC}=3.3V

Single Output Switching & Multiple Outputs Switching Data



C_{LOAD}=50pF
*C_{LOAD}=30pF

Package Availability

	VCX	LCX	LVX	LVT
	CMOS		BiCMOS	
TSSOP (48/56 pin)	●	●	●	●
SSOP (48/56 pin)		●	●	●
TSSOP Type I	●	●	●	●
SSOP Type II (20/24 pin)		●		●
QSOP (20/24 pin)			Note 1	
SOIC JEDEC	●	●	●	●
SOIC EIAJ		●	●	●

Note 1: LVX3245, LVX4245, LVXC3245, LVXC4245

Noise

	V _{OLP} (V)	V _{OLV} (V)
CMOS		
VCX* (16bit) 3.3V	0.4	-0.4
VCX* (16bit) 2.5V	0.3	-0.3
VCX* (16bit) 1.8V	0.2	-0.2
LCX (8bit) 3.3V	0.7	-0.7
LCX (8bit) 2.5V	0.5	-0.5
LCX (16bit) 3.3V	0.4	-0.5
LCX (16bit) 2.5V	0.3	-0.3
LVX (8bit) 3.3V	0.3	-0.3
BiCMOS		
LVT (16bit) 3.3V	0.2	-0.2
LVT (8bit) 3.3V	0.5	-0.5
LVTH (16bit) 2.5V	9.8	-6.3



C_{LOAD}= 50pF, minimum input skew, typical values
*C_{LOAD}=30pF

Note: All values pertain to '16244 function except LVX, which is a '244 function.

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