

# Bourns® Chip Guard®

## ESD Protection Short Form Catalog



*Circuit Protection Solutions*

# Chip Guard® ESD Clamp Protection

Bourns® family of Chip Guard® electrostatic discharge (ESD) protectors is based on a Multi-layer zinc oxide Varistor (MLV) technology. The MLV technology provides excellent electrical performance with a competitive solution for many ESD requirements. The Chip Guard® family is designed to protect sensitive electronic circuits from the threat of ESD to IEC61000-4-2 to level 4 in the ultra-small 0402 and 0603 type packages.

Three Chip Guard® families are available to address key applications. The MLA series has been designed to provide a competitive solution for applications where capacitance of the protector

is less critical. The MLE series has been designed to provide a tolerance on the capacitance of the ESD protector to allow engineers to design the protection into simple first-order filter networks. The MLC family has been designed to provide the engineer with a very low maximum capacitance option of 0.5 pF while still ensuring international standards capability. The three families are manufactured in the MLV technology.

Chip Guard® ESD protection is suitable for a wide variety of applications spanning automotive, computers and support hardware to industrial and consumer products.

## MLA Series: General ESD protection

- IC supply lines
- MOSFET gate protection
- Low frequency digital and control lines
- Computers
- Analog modems
- PDAs

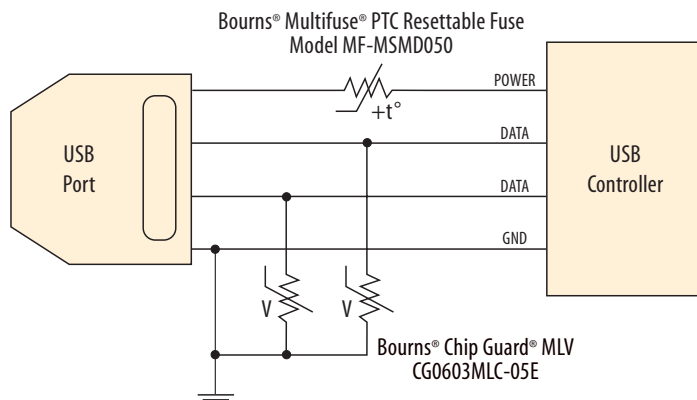
## MLC Series: High speed data and communication ports

- USB 2.0 ports
- IEEE-1394 ports
- SCSI ports
- DVI (Digital Video Interface) ports
- Computers
- Peripherals
- Mobile phones
- Antenna protection

## MLE Series: High speed protection lines

- Ethernet ports
- RS232 ports
- RS485 ports
- POS equipment
- Process controllers
- Medical equipment (excluding critical life support applications)

# Chip Guard® Device in a Typical Application



# Product Selection Guide

## MLA Series

Part Number	Working Voltage		Tolerance	Clamping Voltage	Impulse Current	Capacitance
	V <sub>rms</sub> (V)	V <sub>DC</sub> (V)		V <sub>C</sub> (V)	I <sub>TM</sub> (A) Max.	C <sub>p</sub> (pF) Typical
	<50 µA			1 A @ 8/20 µs	@ 8/20 µs	1 V <sub>rms</sub> @ 1 MHz
CG0402MLA-5.5MG	4	5.5	20 %	19	20	300
CG0402MLA-14KG	11	14	10 %	38	20	100
CG0402MLA-18KG	14	18	10 %	45	20	95
CG0603MLA-5.5ME	4	5.5	20 %	19	30	300
CG0603MLA-14KE	11	14	10 %	35	30	160
CG0603MLA-18KE	14	18	10 %	40	30	140

## MLC Series

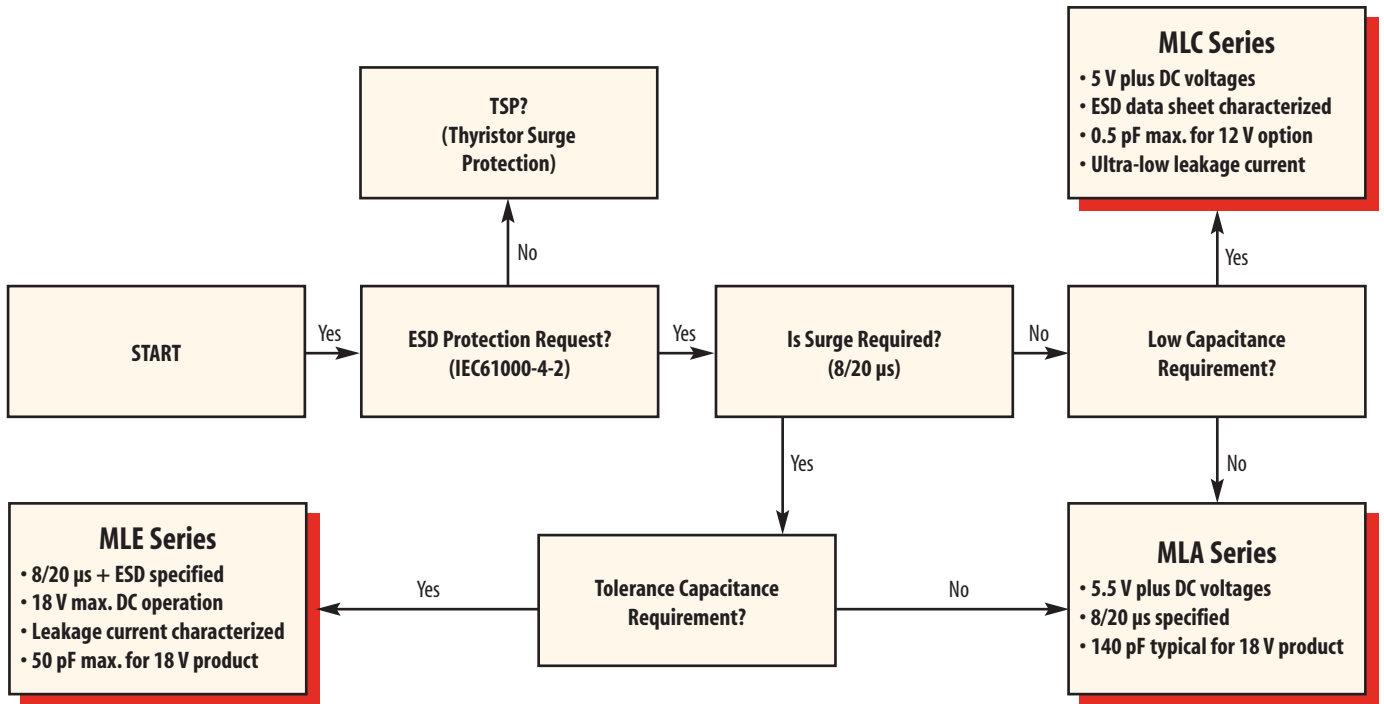
Part Number	Continuous Operating Voltage		Clamping Voltage	Off-state Current	Response Time	Capacitance
	V <sub>DC</sub> (V)		V <sub>CLAMP</sub> (V)	I <sub>L</sub> (nA)	T <sub>D</sub> (ns)	C <sub>OFF</sub> (pF)
	Typ.	Max.	Max.	Max.	Max.	Max.
CG0603MLC-05E	5	6	35	50	1	0.5
CG0603MLC-12E	12		50	50	1	0.5

## MLE Series

Part Number	Continuous Operating Voltage			Clamping Voltage	Off-state Current	Capacitance
	V <sub>rms</sub> (V)	V <sub>DC</sub> (V)		V <sub>CLAMP</sub> (V)	I <sub>L</sub> (µA)	C <sub>p</sub> (pF)
	Max.	Typ.	Max.	Typ.	Max.	Max.
				8 kV Contact	12 V	1 V <sub>rms</sub> @ 1 MHz
CG0402MLE-18G	8.5	12	18	100	1	9
CG0603MLE-18E	8.5	12	18	40	1	50

The family of Chip Guard® electrostatic discharge (ESD) protectors are currently limited to a small range of voltage options. However, the MLV process allows a wider range to be manufactured. Should a voltage that is not highlighted in the current selection be required, please inquire with your local representative as the family will be expanding in the future.

# Chip Guard® Family Selection



## How To Order

**CG 0402 MLA - 5.5 M G**

Chip Guard® Product Designator \_\_\_\_\_

Package Option \_\_\_\_\_  
 • 0402 (MLA, MLE Series)    • 0603 (MLA, MLC, MLE Series)

Multilayer Series Designator \_\_\_\_\_  
 • MLA    • MLC    • MLE

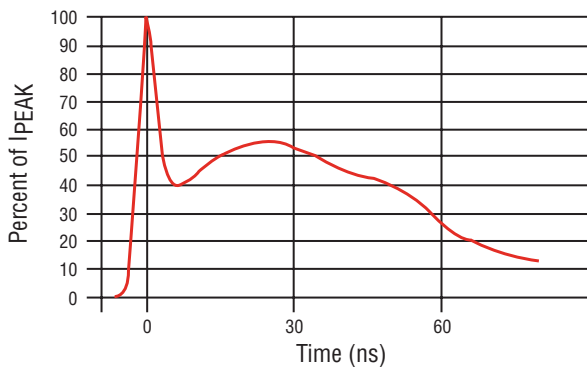
Operating Voltage \_\_\_\_\_  
 • 05 = 5 V (MLC Series)    • 14 = 14 V (MLA Series)  
 • 5.5 = 5.5 V (MLA Series)    • 18 = 18 V (MLA, MLE Series)  
 • 12 = 12 V (MLC Series)

Tolerance (MLA Series Only) \_\_\_\_\_  
 • K = 10 %    • M = 20 %

Tape & Reel Packaging \_\_\_\_\_  
 • E = 4,000 pcs. per reel (MLA and MLE Series)    • E = 5,000 pcs. per reel (MLC Series)    • G = 10,000 pcs. per reel (MLA and MLE Series)

# ESD and Chip Guard® Technology

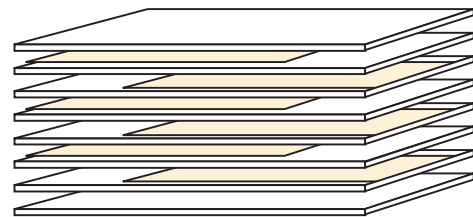
Electrostatic Discharge occurs when a charge is exchanged between two objects of unequal charge potential. ESD, most often between people and metal objects is a result of a build-up of electrons that behave as a capacitor when dielectric isolation is available. Man-made materials such as the sole of a shoe achieve dielectric isolation, while a person walking on carpet creates kinetic energy. The International Electro-technical Commission (IEC) developed a human model ESD event that allows designers to take adequate protection in their electrostatic applications. The IEC defined the ESD discharge impulse with a rise time of less than 1 ns and decay time of 60 ns as highlighted in the graph below. The new standard, IEC61000-4-2 identifies four levels.



Integrated Circuit (IC) manufacturers of electrostatic sensitive devices design a level of protection into the IC to increase its robustness. However, protection circuits add cost to the device by consuming expensive silicon real estate. IC manufacturers design to standards to protect against board manufacturing processes such as IEC61000-4-2 Level 1, a 2 kV contact voltage. However, human body ESD voltages are nature-determined and can be 15 kV or more which will damage the IC. IEC61000-4-2; Level 4 specifies an air discharge up to 15 kV to take this into consideration. It is common practice to protect all “people-interactive” data ports to Level 4, thereby limiting product damage and increasing the robustness of the equipment. Therefore, the

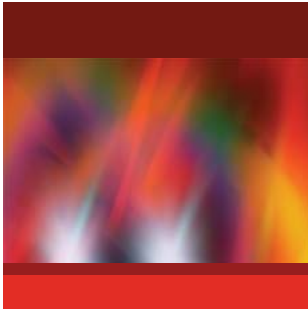
external ESD protector becomes the first level of protection with the IC providing residual second level protection in the design.

Bourns® ChipGuard® Multilayer Varistors are manufactured by layering zinc oxide ceramics between metal electrodes. Each metal oxide ceramic layer has a defined breakdown voltage that is placed in series and defines the voltage rating of the device. The current handling capability is determined by the size of the metal oxide layer plate. As the voltage reaches its designed maximum, the oxide level transitions from the normal high impedance state to a low impedance and behaves like a voltage clamp to the overvoltage impulse. As each oxide plate is in series, the effective capacitance is reduced, making them suitable for high-speed communication ports as well as robust enough for IC dc power lines.



Communication port frequencies are continually increasing for external peripherals and networks. USB 1.1 specified a maximum of 12 Mbps while the latest USB 2.0 specifies 480 Mbps. Coupled with “hot swapping” capability with power feed, the USB port is a hostile environment. The MLC family has been designed to address high-speed communication ports while meeting IEC61000-4-2 to Level 4. A maximum capacitance of 0.5 pF limits signal distortion while low leakage currents of 50 nA ensures a low drain on battery-powered applications. The voltage feed line can be protected with the MLA series and a resettable overcurrent limit using Bourns® MF-MSMD & MF-USMD Multifuse® Polymer PTCs.

IEC61000-4-2 Level	Contact Voltage (kV)	Air Discharge Voltage (kV)	Peak Contact Current (A)	Contact Current @ 30 ns (A)	Contact Current @ 60 ns (A)
Level 1	2	2	7.5	4	2
Level 2	4	4	15	8	4
Level 3	6	8	22.5	12	6
Level 4	8	15	30	16	8



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[www.bourns.com](http://www.bourns.com)

Bourns® products are available through an extensive network of manufacturer's representatives, agents and distributors. To obtain technical applications assistance, a quotation, or to place an order, contact a Bourns representative in your area.



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