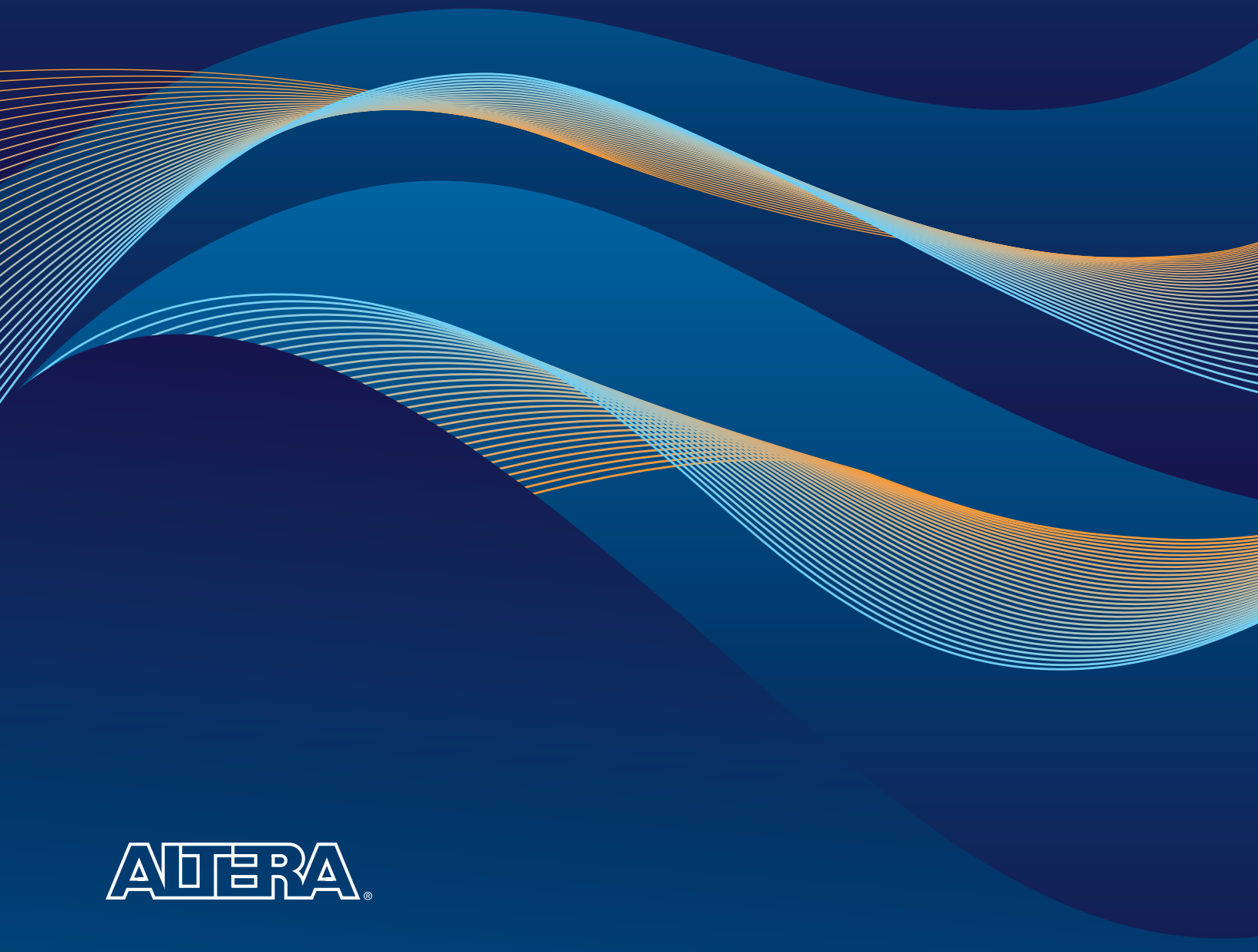
Version 11.1

Altera Product Catalog



Contents

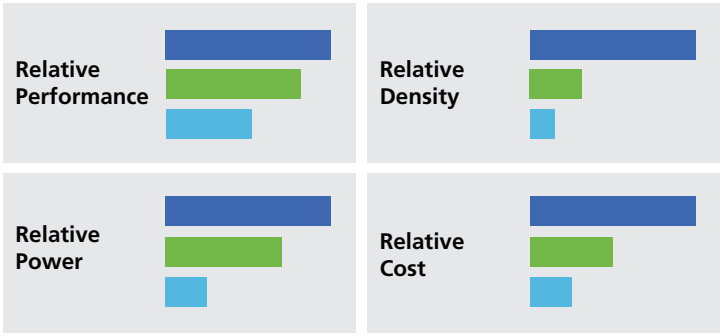
Altera delivers the broadest portfolio of custom logic devices—FPGAs, SoC FPGAs, ASICs, and CPLDs. This uniquely positions us to bring your great ideas to life faster, better, and more cost effectively. You can count on it.

FPGAs

Altera® FPGAs give you the best performance, the lowest power, and the widest range of densities. We have three classes of FPGAs to meet your needs, all optimized for value. Our flagship Stratix series delivers the industry's highest density and performance FPGAs, while our Arria series is perfect for high-performance computation functionality and keeping costs down. Choose the Cyclone series for the lowest power and cost in high-volume, cost-sensitive applications.

SoC FPGAs

SoC FPGA devices, the newest members of the Cyclone V and Arria V families, consolidate two discrete devices into one, reducing system power, cost, and board size while increasing performance. SoC FPGAs integrate an ARM-based hard processor system (HPS) consisting of a dual-core ARM® processor, peripherals, and memory controllers with the FPGA fabric using a high-bandwidth interconnect backbone. We include a wide range of system peripherals, Altera intellectual property (IP), custom IP, and third-party IP that lets you quickly create a custom system using Altera design tools.



Stratix V FPGAs
Highest performance designs, highest logic- and memory-density designs, and ASIC prototyping

Arria V FPGAs
Cost-sensitive applications that require high-performance computation functionality such as digital signal processing (DSP)

Cyclone V FPGAs
High-volume applications at the lowest cost and lowest power

ASICs

If you are looking for an ASIC, stop here. Prototype your designs with our Stratix series FPGAs. Then take advantage of a seamless path to HardCopy series ASICs for volume production. You'll benefit from the shortest time to market, lowest risk, and lowest overall ASIC development costs.

CPLDs

For glue logic and any control functions, our non-volatile MAX series comprises the market's lowest cost CPLDs—a single-chip solution, great for interface bridging, level shifting, I/O expansion, or management of analog I/Os.

Productivity-Enhancing Design Software, Embedded Processing, IP, and Development Kits

With Altera, you get a complete design environment and a wide choice of design tools – all built to work together easily so your designs are up and running fast. You can try one of our training classes to get a jump start on your designs. Choose Altera and see how we will enhance your productivity and make a difference to your bottom line.

Turn the page to get the specification overview of our latest FPGAs, ASICs, and CPLDs, as well as our extended line of products and services. Our broad product portfolio ensures you get the complete and best design solution.

Glossary

Below is a glossary of helpful terms to bring you up to speed on Altera devices.

Term	Definition
Adaptive logic module (ALM)	Logic building block, used by some Altera devices, which provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two combinational adaptive LUTs (ALUTs).
Configuration via Protocol (CvP)	CvP is a configuration method that enables you to configure the FPGA using industry-standard protocols. Currently CvP supports only the PCI Express® (PCIe®) protocol.
Embedded HardCopy Blocks	These metal-programmable hard IP blocks deliver up to 14M ASIC gates or up to 700K additional logic elements (LEs) to harden standard or logic-intensive applications.
Equivalent LE	Device density represented as a comparable amount of LEs, which uses the 4-input LUT as a basis.
Fractional phase-locked loops (fPLL)	A phase-locked loop (PLL) in the core fabric, fPLLs provide increased flexibility as an additional clocking source for the transceiver, replacing external voltage-controlled crystal oscillators (VCXOs).
Global clock networks	Global clocks can drive throughout the entire device, serving as low-skew clock sources for functional blocks such as ALMs, DSP blocks, TriMatrix memory blocks, and PLLs. See regional clocks and periphery clocks for more clock network information.
Hard processor system (HPS)	This processor system is a hardened component within the SoC FPGA which comprises a dual-core ARM Cortex™-A9 MPCore™ processor, a rich set of peripherals, and multiport memory controllers.
LE	Logic building block, used by some Altera devices, that includes a 4-input LUT, a programmable register, and a carry chain connection. See device handbooks for more information.
Macrocells	Similar to LEs, this is the measure of density in MAX series CPLDs.
Memory logic array blocks (MLABs)	MLABs are dual-purpose blocks, configurable as regular logic array blocks or as memory blocks.
On-chip termination (OCT)	Support for driver impedance matching and series termination, which eliminates the need for external resistors, improves signal integrity, and simplifies board design. On-chip series, parallel, and differential termination resistors are configurable via Quartus II software.
Periphery clocks (PCLKs)	PCLKs are a collection of individual clock networks driven from the periphery of the device. PCLKs can be used instead of general-purpose routing to drive signals into and out of the device.
Plug & Play Signal Integrity	This capability, consisting of Altera's adaptive dispersion engine and hot socketing, lets you change the position of backplane cards on the fly, without having to manually configure your backplane equalization settings.
Programmable Power Technology	This feature automatically optimizes logic, DSP, and memory blocks for the lowest power at the required performance. Only the blocks with critical-path logic need to be in high-performance mode; all others are in low-power mode.
Real-time in-system programming (ISP)	This capability allows you to program a MAX II device while the device is still in operation. The new design only replaces the existing design when there is a power cycle to the device. This way, you can perform in-field updates to the MAX II device at any time without affecting the operation of the whole system.
Regional clocks	Regional clocks are device quadrant-oriented and provide the lowest clock delay and skew for logic contained within a single device quadrant.
System on a chip (SoC)	An SoC is an embedded system that consists of a processor, peripherals, and custom hardware integrated on a single device.
Variable-precision DSP blocks	These integrated blocks provide native support for signal processing of varying precisions—for example, 9x9, 27x27, and 18x36—in a sum or independent mode.

www.altera.com/selector

Stratix V GT FPGA Features

The following features, packages, and I/O matrices give you an overview of our devices. To get the full story, check out our online selector guide: www.altera.com/selector.

		Stratix V GT FPGAs (0.85 V), Up to 28.05-Gbps Transceivers[1]	
		5SGTC5	5SGTC7
Density and Speed	ALMs	160,400	234,720
	Equivalent LEs	425,000	622,000
	Registers[2]	641,600	938,880
	M20K memory blocks	2,304	2,560
	M20K memory (Mb)	45	50
	MLAB memory (Mb)	4.9	7.16
	18-bit x 18-bit multipliers	512	512
	27-bit x 27-bit DSP blocks	256	256
	Speed grades: FPGA fabric (fastest to slowest)	-2, -3	
	Speed grades: transceiver (fastest to slowest)	-2, -3, -4	
Architectural Features	Global clock networks	16	
	Regional clock networks	92	
	Design security	✓	
	HardCopy series device support	Contact Altera	
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]	
	I/O standards supported	LVTTL, LVCMOS, PCI™, PCI-X™, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-5, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)	
	LVDS channels, 1.4 Gbps (receive/transmit)	150	150
	Embedded DPA circuitry	✓	
	Series, parallel, and differential OCT	✓	
	Transceiver (SERDES) channels (28.05 Gbps/14.1 Gbps)	4/32	4/32
	PCIe Gen3 hard IP blocks	1	1
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR	

[1] All data is preliminary.

[2] 3.3-V compliant, requires a 3-V power supply.

Stratix V GX FPGA Features

		Stratix V GX FPGAs (0.85 V), Up to 14.1-Gbps Transceivers[1]							
		5SGXA3	5SGXA4	5SGXA5	5SGXA7	5SGXA9	5SGXAB	5SGXB5	5SGXB6
Density and Speed	ALMs	128,300	158,500	185,000	234,720	317,000	359,200	185,000	225,400
	Equivalent LEs	340,000	420,000	490,000	622,000	840,000	952,000	490,000	597,000
	Registers[2]	513,200	634,000	740,000	938,880	1,268,000	1,436,800	740,000	901,600
	M20K memory blocks	957	1,900	2,304	2,560	2,640	2,640	2,100	2,660
	M20K memory (Mb)	19	37	45	50	52	52	41	52
	MLAB memory (Mb)	3.92	4.84	5.65	7.16	9.67	10.96	5.65	6.88
	18-bit x 18-bit multipliers	512	512	512	512	704	704	798	798
	27-bit x 27-bit DSP blocks	256	256	256	256	352	352	399	399
	Speed grades: FPGA fabric (fastest to slowest)	-2, -3, -4							
	Speed grades: transceiver (fastest to slowest)	-1, -2, -3							
Architectural Features	Global clock networks	16							
	Regional clock networks	92							
	Design security	✓							
	HardCopy series device support	✓							
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]							
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-5, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)							
	LVDS channels, 1.4 Gbps (receive/transmit)	174	174	210	210	210	210	150	150
	Embedded DPA circuitry	✓							
	Series, parallel, and differential OCT	✓							
	Transceiver (SERDES) channels (14.1 Gbps)	36	36	48	48	48	48	66	66
	PCIe Gen3 hard IP blocks	1 or 2	1 or 2	1,2, or 4	1,2, or 4	1,2, or 4	1,2, or 4	1 or 4	1 or 4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR							

[1] All data is preliminary.

[2] 3.3-V compliant, requires a 3-V power supply.

Stratix V GS FPGA Features

		Stratix V GS FPGAs (0.85 V), Up to 14.1-Gbps Transceivers[1]				
		5SGSD3	5SGSD4	5SGSD5	5SGSD6	5SGSD8
Density and Speed	ALMs	89,000	135,840	172,600	220,000	262,400
	Equivalent LEs	236,000	360,000	457,000	583,000	695,000
	Registers[2]	356,000	543,360	690,400	880,000	1,049,600
	M20K memory blocks	688	957	2,014	2,320	2,567
	M20K memory (Mb)	13	19	39	45	50
	MLAB memory (Mb)	2.72	4.15	5.27	6.71	8.01
	18-bit x 18-bit multipliers	1,200	2,088	3,180	3,550	3,926
	27-bit x 27-bit DSP blocks	600	1,044	1,590	1,775	1,963
	Speed grades: FPGA fabric (fastest to slowest)	-2, -3, -4				
	Speed grades: transceiver (fastest to slowest)	-1, -2, -3				
Architectural Features	Global clock networks	16				
	Regional clock networks	92				
	Design security	✓				
	HardCopy series device support	✓				
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]				
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-5, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)				
	LVDS channels, 1.4 Gbps (receive/transmit)	108	174	174	210	210
	Embedded DPA circuitry	✓				
	Series, parallel, and differential OCT	✓				
	Transceiver (SERDES) channels (14.1 Gbps)	24	36	36	48	48
	PCIe Gen3 hard IP blocks	1	1	1	1 or 2	1 or 2
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR				

[1] All data is preliminary.

[2] 3.3-V compliant, requires a 3-V power supply.

Stratix V E FPGA Features

		Stratix V E FPGAs (0.85 V)[1]	
		5SEE9	5SEEB
Density and Speed	ALMs	317,000	359,200
	Equivalent LEs	840,000	952,000
	Registers[2]	1,268,000	1,436,800
	M20K memory blocks	2,640	2,640
	M20K memory (Mb)	52	52
	MLAB memory (Mb)	9.67	10.96
	18-bit x 18-bit multipliers	704	704
	27-bit x 27-bit DSP blocks	352	352
	Speed grades: FPGA fabric (fastest to slowest)	-3, -4	
Architectural Features	Global clock networks	16	
	Regional clock networks	92	
	Design security	✓	
	HardCopy series device support	✓	
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]	
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-5, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)	
	LVDS channels, 1.4 Gbps (receive/transmit)	210	210
	Embedded DPA circuitry	✓	
	Series, parallel, and differential OCT	✓	
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR	

[1] All data is preliminary.

[2] 3.3-V compliant, requires a 3-V power supply.

Stratix IV GT FPGA Features

		Stratix IV GT FPGAs (0.95 V), 11.3-Gbps Transceivers[1]					
		EP4S40G2	EP4S40G5	EP4S100G2	EP4S100G3	EP4S100G4	EP4S100G5
Density and Speed	ALMs	91,200	212,480	91,200	116,480	141,440	212,480
	Equivalent LEs	228,000	531,200	228,000	291,200	353,600	531,200
	Registers[2]	182,400	424,960	182,400	232,960	282,880	424,960
	M9K memory blocks	1,235	1,280	1,235	936	1,248	1,280
	M144K memory blocks	22	64	22	36	48	64
	MLAB memory (Kb)	2,850	6,640	2,850	3,640	4,420	6,640
	Embedded memory (Kb)	14,283	20,736	14,283	13,608	18,144	20,736
	18-bit x 18-bit multipliers	1,288	1,024	1,288	832	1,024	1,024
	Speed grades (fastest to slowest)	-1, -2, -3					
Architectural Features	Global clock networks	16					
	Regional clock networks	64	88	64	88	88	88
	Periphery clock networks	88	112	88	112	112	112
	PLLs/unique outputs	8/68	8/68	8/68	12/96	12/96	12/96
	Design security	✓					
	HardCopy series device support	–					
	Configuration file size (Mb)	95	172	95	172	172	172
	Others	Plug & Play Signal Integrity, Programmable Power Technology					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)					
	Emulated LVDS channels, 1,100 Mbps	192	256	192	256	256	256
	LVDS channels, 1,600 Mbps (receive/transmit)	46/46					
	Embedded DPA circuitry	✓					
	Series, parallel, and differential OCT	✓					
	Transceiver (SERDES) channels[4] (11.3 Gbps/8.5 Gbps/6.5 Gbps)	12/12/12	12/12/12	24/0/12	24/8/16	24/8/16	32/0/16
	PCIe hard IP blocks	2	2	2	4	4	4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR					

[1] Available in industrial temperatures only (0°C to 100°C).

[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

[3] 3.3-V compliant, requires a 3-V power supply.

[4] The total transceiver count is the sum of 11.3-Gbps plus 8.5-Gbps plus 6.5-Gbps transceivers.

Stratix IV GX FPGA Features

		Stratix IV GX FPGAs (0.9 V), 8.5-Gbps Transceivers[1]						
		EP4SGX70	EP4SGX110	EP4SGX180	EP4SGX230	EP4SGX290	EP4SGX360	EP4SGX530
Density and Speed	ALMs	29,040	42,240	70,300	91,200	116,480	141,440	212,480
	Equivalent LEs	72,600	105,600	175,750	228,000	291,200	353,600	531,200
	Registers[2]	58,080	84,480	140,600	182,400	232,960	282,880	424,960
	M9K memory blocks	462	660	950	1,235	936	1,248	1,280
	M144K memory blocks	16	16	20	22	36	48	64
	MLAB memory (Kb)[2]	908	1,320	2,197	2,850	3,640	4,420	6,640
	Embedded memory (Kb)	6,462	8,244	11,430	14,283	13,608	18,144	20,736
	18-bit x 18-bit multipliers	384	512	920	1,288	832	1,040[3]	1,024
	Speed grades (fastest to slowest)	-2, -2x[4], -3, -4	-2, -2x[4], -3, -4	-2, -2x[4], -3, -4	-2, -2x[4], -3, -4	-2, -2x[4], -3, -4	-2, -2x[4], -3, -4	-2, -3, -4
Architectural Features	Global clock networks	16						
	Regional clock networks	64	64	64	64	88	88	88
	Periphery clock networks	56	56	88	88	88	88	112
	PLLs/unique outputs	4/34	4/34	8/68	8/68	12/96	12/96	12/96
	Design security	✓						
	HardCopy series device support	✓[5]	✓[5]	✓	✓	✓	✓	✓
	Configuration file size (Mb)	53	53	95	95	141	141	172
	Others	Plug & Play Signal Integrity, Programmable Power Technology						
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[6]						
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)						
	Emulated LVDS channels, 1,100 Mbps	128	128	192	192	256	256	256
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	56/56	88/88	88/88	98/98	98/98	98/98
	Embedded DPA circuitry							
	Series, parallel, and differential OCT	✓						
	Transceiver (SERDES) channels (8.5 Gbps/6.5 Gbps)[7]	16/8	16/8	24/12	24/12	32/16	32/16	32/16
	PCIe hard IP blocks	2	2	2	2	4	4	4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR						

[1] Maximum LVDS channels, transceiver channels, PLLs/unique outputs, and PCIe hard IP blocks for the product line shown.Various packages offer a variety of options to meet your design needs.

[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50 percent.

[3] EP4SGX360N has 1,024 18x18 multipliers.

[4] Support for -2 core and -3 I/O speed-grade. Support for PCIe Gen1 and Gen2 x8. Selected devices only.

[5] For EP4SGX70D and EP4SGX110D/F devices.

[6] 3.3-V compliant, requires a 3-V power supply.

[7] The total transceiver count is the sum of 8.5-Gbps transceivers plus 6.5-Gbps transceivers.

Stratix IV E FPGA Features

		Stratix IV E FPGAs (0.9 V)			
		EP4SE230	EP4SE360	EP4SE530	EP4SE820
Density and Speed	ALMs	91,200	141,440	212,480	325,220
	Equivalent LEs	228,000	353,600	531,200	813,050
	Registers[1]	182,400	282,880	424,960	650,440
	M9K memory blocks	1,235	1,248	1,280	1,610
	M144K memory blocks	22	48	64	60
	MLAB memory (Kb)	2,850	4,420	6,640	10,163
	Embedded memory (Kb)	14,283	18,144	20,736	23,130
	18-bit x 18-bit multipliers	1,288	1,040	1,024	960
	Speed grades (fastest to slowest)	-2, -3, -4	-2, -3, -4	-2, -3, -4	-3, -4
Architectural Features	Global clock networks	16			
	Regional clock networks	64	88	88	88
	Periphery clock networks	88	88	112	132
	PLLs/unique outputs	4/34	12/96	12/96	12
	Design security	✓			
	Configuration file size (Mb)	95	141	172	230
	HardCopy series device support	✓			
	Others	Programmable Power Technology			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)			
	Emulated LVDS channels, 1,100 Mbps	128	256	256	288
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	88/88	112/112	132/132
	Embedded DPA circuitry	✓			
	Series, parallel, and differential OCT	✓			
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR			

[1] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which can increase the total register count by an additional 50 percent.

[2] 3.3-V compliant, requires a 3-V power supply.

Stratix III L FPGA Features

		Stratix III L FPGAs (1.1 V, 0.9 V)					
		EP3SL50	EP3SL70	EP3SL110	EP3SL150	EP3SL200	EP3SL340
Density and Speed	ALMs	19,000	27,000	42,600	56,800	79,560	135,200
	Equivalent LEs	47,500	67,500	107,500	142,500	198,900	338,000
	Registers[1]	38,000	54,000	85,200	113,600	159,120	270,400
	M9K memory blocks	108	150	275	355	468	1,040
	M144K memory blocks	6	6	12	16	36	48
	MLAB memory (Kb)[2]	297	422	672	891	1,250	2,110
	Embedded memory (Kb)	1,836	2,214	4,203	5,499	9,396	16,272
	18-bit x 18-bit multipliers	216	288	288	384	576	576
	Speed grades (fastest to slowest)	-2, -3, -4					
Architectural Features	Global clock networks	16					
	Regional clock networks	48	48	48	48	88	88
	Periphery clock networks	104	104	208	208	208	208
	PLLs/unique outputs	4/34	4/34	8/68	8/68	12/96	12/96
	Design security	✓					
	Configuration file size (Mb)	22	22	47	47	66	120
	HardCopy series device support	✓					
	Others	Programmable Power Technology					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3					
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS					
	Emulated LVDS channels, 1,100 Mbps	56	56	88	88	112	137
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	56/56	88/88	88/88	112/112	132/132
	Embedded DPA circuitry	✓					
	Series, parallel, and differential OCT	✓					
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR					

[1] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50 percent.
[2] The size of the MLAB ROM is twice the size of the MLAB RAM.

Stratix III E FPGA Features

		Stratix III E FPGAs (1.1 V)			
		EP3SE50	EP3SE80	EP3SE110	EP3SE260
Density and Speed	ALMs	19,000	32,000	42,600	101,760
	Equivalent LEs	47,500	80,000	107,500	254,400
	Registers[1]	38,000	64,000	85,200	203,520
	M9K memory blocks	400	495	639	864
	M144K memory blocks	12	12	16	48
	MLAB memory (Kb)[2]	297	500	672	1,594
	Embedded memory (Kb)	5,328	6,183	8,055	14,688
	18-bit x 18-bit multipliers	384	672	896	768
	Speed grades (fastest to slowest)	-2, -3, -4			
Architectural Features	Global clock networks	16			
	Regional clock networks	48	48	48	88
	Periphery clock networks	104	208	208	208
	PLLs/unique outputs	4/34	8/68	8/68	12/96
	Design security	✓			
	Configuration file size (Mb)	26	48	48	93
	HardCopy series device support	✓			
	Others	Programmable Power Technology			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS			
	Emulated LVDS channels, 1,100 Mbps	56	88	88	112
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	88/88	88/88	112/112
	Embedded DPA circuitry	✓			
	Series, parallel, and differential OCT	✓			
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR			

[1] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50 percent.
[2] The size of the MLAB ROM is twice the size of the MLAB RAM.

Stratix II GX FPGA Features

		Stratix II GX FPGAs (1.2 V), 6.375-Gbps Transceivers[1]			
		EP2SGX30	EP2SGX60	EP2SGX90	EP2SGX130
Density and Speed	ALMs	13,552	24,176	36,384	53,016
	Equivalent LEs	33,880	60,440	90,960	132,540
	Registers[2]	27,104	48,352	72,708	106,032
	M512 memory blocks	202	329	488	699
	M4K memory blocks	144	255	408	609
	M512K memory blocks	1	2	4	6
	Embedded memory (Kb)	1,338	2,485	4,415	6,590
	18-bit x 18-bit multipliers	64	144	192	252
	Speed grades (fastest to slowest)	-3, -4, -5			
Architectural Features	Global clock networks	48			
	Regional clock networks	48			
	PLLs/unique outputs	4/18	8/36	8/36	8/36
	Design security	✓			
	Configuration file size (Mb)	10	17	28	40
	HardCopy series device support	–	–	–	–
	Others	Plug & Play Signal Integrity			
I/O Features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVDS, LVPECL, HyperTransport™, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS			
	LVDS channels, 1,000 Mbps (receive/transmit)	31/29	42/42	59/59	73/71
	Embedded DPA circuitry	✓			
	Series and differential OCT	✓			
	Transceiver (SERDES) channels (6.375 Gbps)	8	12	16	20
	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR			

[1] Maximum PLLs/unique outputs, LVDS channels, and transceiver channels for the product line shown. Various packages offer a variety of options to meet your design needs.

[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50 percent.

Stratix FPGA Series Package and I/O Matrices

	Stratix V GS, GX, GT, and E FPGAs (0.85 V), Up to 28.05-Gbps Transceivers						
	FBGA (F)						
	780 pin 29 x 29 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch	**1,760 pin** 42.5 x 42.5 (mm) 1.0-mm pitch	**1,932 pin** 45 x 45 (mm) 1.0-mm pitch
5SGSD3	360, 90, 12[1]	432, 108, 24					
5SGSD4	360, 90, 12[1]	432, 108, 24		696, 174, 36			
5SGSD5		552, 138, 24		696, 174, 36			
5SGSD6				696, 174, 36			840, 210, 48
5SGSD8				696, 174, 36			840, 210, 48
5SGXA3	360, 90, 12[1]	432, 108, 24	432, 108, 36	696, 174, 36			
5SGXA4		552, 138, 24	432, 108, 36	696, 174, 36			
5SGXA5		552, 138, 24	432, 108, 36	696, 174, 36	600, 150, 48		840, 210, 48
5SGXA7		552, 138, 24	432, 108, 36	696, 174, 36	600, 150, 48		840, 210, 48
5SGXA9				696, 174, 36[2]			840, 210, 48
5SGXAB				696, 174, 36[2]			840, 210, 48
5SGXB5				432, 108, 66		600, 150, 66	
5SGXB6				432, 108, 66		600, 150, 66	
5SGTC5					600, 150, 36[3]		
5SGTC7					600, 150, 36[3]		
5SEE9				696, 174, 0[2]			840, 210, 0
5SEEB				696, 174, 0[2]			840, 210, 0

[1] Hybrid package (flip chip) FBGA: 33 x 33 (mm) 1.0-mm pitch.
[2] Hybrid package (flip chip) FBGA: 45 x 45 (mm) 1.0-mm pitch.
[3] GX–GT migration. Unused transceiver channels connected to power/ground.

264, 66, 24 Numbers indicate GPIO count, LVDS count, and transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). User I/Os may be less than labelled for vertical migration.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0˚C to 100˚C).

Stratix Series Package and I/O Matrices

	Stratix IV GT FPGAs (0.95 V), 11.3-Gbps Transceivers	
	FBGA (F)[1]	
	1,517 pin 40 x 40 (mm) 1.0-mm pitch	**1,932 pin** 45 x 45 (mm) 1.0-mm pitch
EP4S40G2	646 12+12+12	
EP4S40G5	646[2] 12+12+12	
EP4S100G2	646 24+0+12	
EP4S100G3		769 24+8+16
EP4S100G4		769 24+8+16
EP4S100G5	646[2] 24+0+12	769 32+0+16

[1] FineLine ball grid array.

[2] Hybrid package (flip chip) FBGA: 42.5 x 42.5 (mm) 1.0-mm pitch.

636 (12+12+12) Values on top indicate available user I/O pins; values on bottom indicate the 11.3-Gbps plus 8.5-Gbps plus 6.5-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0˚C to 100˚C).

	Stratix IV GX FPGAs (0.9 V), 8.5-Gbps Transceivers[1]					
	FBGA (F)					
	780 pin 29 x 29 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch	**1,760 pin** 42.5 x 42.5 (mm) 1.0-mm pitch	**1,932 pin** 45 x 45 (mm) 1.0-mm pitch
EP4SGX70	368 8+0		480 16+8			
EP4SGX110	368 8+0	368 16+0	480 16+8			
EP4SGX180	368 8+0	560 16+0	560 16+8	736 24+12		
EP4SGX230	368 8+0	560 16+0	560 16+8	736 24+12		
EP4SGX290	288[2] 16+0	560 16+0	560 16+8	736 24+12	864 24+12	904 32+16
EP4SGX360	288[2] 16+0	560 16+0	560 16+8	736 24+12	864 24+12	904 32+16
EP4SGX530			560[3] 16+8	736[3] 24+12	864 24+12	904 32+16

[1] I/O counts do not include dedicated clock inputs that can be used as data inputs.

[2] Hybrid package (flip chip) FBGA: 35 x 35 (mm) 1.0-mm pitch.

[3] Hybrid package (flip chip) FBGA: 42.5 x 42.5 (mm) 1.0-mm pitch.

636 (8+0) Values on top indicate available user I/O pins; values at the bottom indicate the 8.5-Gbps plus 6.5-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0˚C to 100˚C).

Stratix Series Package and I/O Matrices

		FBGA (F)				
		484 pin 23 x 23 (mm) 1.0-mm pitch	**780 pin** 29 x 29 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch	**1,760 pin** 42.5 x 42.5 (mm) 1.0-mm pitch
Stratix IV E FPGAs	**EP4SE820**			736[3]	960[3]	1,104
	EP4SE530			736[3]	960[3]	960
	EP4SE360		480[2]	736		
	EP4SE230		480			
Stratix III E FPGAs[1]	**EP3SE260[3]**		480[2]	736	960	
	EP3SE110		480	736		
	EP3SE80		480	736		
	EP3SE50	288	480			
Stratix III L FPGAs[1]	**EP3SL340**			736[3]	960	1,104
	EP3SL200		480[2]	736	960	
	EP3SL150		480	736		
	EP3SL110		480	736		
	EP3SL70	288	480			
	EP3SL50	288	480			

[1] I/O counts do not include dedicated clock inputs that can be used as data inputs.
[2] Hybrid package (flip chip) FBGA: 35 x 35 (mm) 1.0-mm pitch.
[3] Hybrid package (flip chip) FBGA: 42.5 x 42.5 (mm) 1.0-mm pitch.

288 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0°C to 100°C).

	Stratix II GX FPGAs (1.2 V), 6.35-Gbps Transceivers[1]		
	FBGA (F)		
	780 pin 29 x 29 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,508 pin** 40 x 40 (mm) 1.0-mm pitch
EP2SGX30	361 8		
EP2SGX60	364 8	534 12	
EP2SGX90		558 12	650 16
EP2SGX130			734 20

[1] I/O counts do not include dedicated clock inputs that can be used as data inputs.

636 / 12 Values on top indicate available user I/O pins; values on bottom indicate the 6.35-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0°C to 100°C).

HardCopy IV ASIC Features

		HardCopy IV ASICs (0.9 V), 6.5-Gbps Transceivers				
		HC4GX15	HC4GX25	HC4GX35	HC4E25	HC4E35
Density and Speed	Usable ASIC gates	9.4M	11.5M	11.5M	9.4M	14.6M
	Equivalent LEs	353,600	531,600	531,600	353,600	813,050
	M9K memory blocks	660	936	1,280	864	1,320
	M144K memory blocks	24	36	64	32	48
	MLAB memory	Implemented in HCells				
	Embedded memory (Kb)	9,396	13,608	20,736	12,384	18,792
	18-bit x 18-bit multipliers[1]	1,288	1,288	1,288	1,288	1,040
Architectural Features	PLLs/unique outputs	3/27	6/54	8/68	4/34	12/96
	Design security[2]			✓		
	Stratix series prototyping support	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360	EP4SGX110 EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530	EP4SGX180 EP4SGX230 EP4SGX290 EP4SGX360 EP4SGX530	EP4SE230 EP4SE360	EP4SE360 EP4SE530 EP4SE820
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]				
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2,Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)				
	Emulated LVDS channels, 1,100 Mbps	184	236	280	120	216
	LVDS channels, 1,250 Mbps (receive/transmit)	28/28	44/44	88/88	56/56	88/88
	Embedded DPA circuitry			✓		
	Series and differential OCT			✓		
	Transceiver (SERDES) channels (6.5 Gbps/6.5 Gbps, PMA only)	8/0	16/8	24/12	—	—
	PCIe hard IP blocks	1	2	2	—	—
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR				

[1] Implemented in HCells.

[2] Since all HardCopy ASICs contain hard-wired logic, they are inherently secure.

[3] 3.3-V compliant, requires a 3-V power supply.

HardCopy III ASIC Features

		HardCopy III ASICs (0.9 V)	
		HC325	HC335
Density and Speed	Usable ASIC gates	7.0M	7.0M
	Equivalent LEs	338,000	338,000
	M9K memory blocks	864	1,040
	M144K memory blocks	32	48
	MLAB memory	Implemented in HCells	
	Embedded memory (Kb)	12,384	16,272
	18-bit x 18-bit multipliers[1]	896	1,040
Architecural Features	PLLs/unique outputs	8/68	12/96
	Design security[2]	✓	
	Stratix series prototyping support	EP3SE110 EP3SL110 EP3SL150 EP3SL200 EP3SE260 EP3SL340	EP3SE110 EP3SL150 EP3SL200 EP3SE260 EP3SL340
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]	
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)	
	Emulated LVDS channels, 1,100 Mbps	120	216
	LVDS channels, 1,250 Mbps (receive/transmit)	56/56	88/88
	Embedded DPA circuitry	✓	✓
	Series and differential OCT	✓	
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR	

[1] Implemented in HCells.

[2] Since all HardCopy ASICs contain hard-wired logic, they are inherently secure.

[3] 3.3-V compliant, requires a 3-V power supply.

HardCopy II ASIC Features

		HardCopy II ASICs				
		HC210W	**HC210**	**HC220**	**HC230**	**HC240**
Density and Speed	Usable ASIC gates	1.0M	1.0M	1.9M	2.9M	3.6M
	Equivalent LEs	90,960	90,960	132,540	179,400	179,400
	M512 memory blocks	Not available in HardCopy II ASICs				
	M4K memory blocks	190	190	408	614	768
	M512K memory blocks	0	0	2	6	9
	Embedded memory (Kb)	855	855	2,988	6,219	8,640
	18-bit x 18-bit multipliers[1]	192	192	252	384	384
Architectural Features	PLLs/unique outputs	4/32	4/32	4/32	8/64	12/88
	Design security[2]	✓				
	Stratix series prototyping support	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90	EP2S60 EP2S90 EP2S130	EP2S90 EP2S130 EP2S180	EP2S180
I/O Features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X 1.0, LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HyperTransport				
	LVDS channels, 1,040 Mbps (receive/transmit)	17/13	21/19	30/29	46/44	116/116
	Embedded DPA circuitry	✓				
	Series and differential OCT	✓				
External Memory Interfaces	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR				

[1]Implemented in HCells.

[2]Since all HardCopy ASICs contain hard-wired logic, they are inherently secure.

HardCopy Series Package and I/O Matrices

	HardCopy IV ASICs (0.9 V), 6.5-Gbps Transceivers							
	FBGA (F)							
	484 (WF[1]) 23 x 23 (mm) 1.0-mm pitch	**484 (FF[2])** 23 x 23 (mm) 1.0-mm pitch	**780 (WF)** 29 x 29 (mm) 1.0-mm pitch	**780 (LF[3])** 29 x 29 (mm) 1.0-mm pitch	**780 (FF)** 29 x 29 (mm) 1.0-mm pitch	**1,152 (LF)** 35 x 35 (mm) 1.0-mm pitch	**1,152 (FF)** 35 x 35 (mm) 1.0-mm pitch	**1,517 (FF)** 40 x 40 (mm) 1.0-mm pitch
HC4GX15				372 8+0				
HC4GX25				289 16+0		564 16+0	564 16+8	
HC4GX35							564 16+8	744 24+12
HC4E25	296	296	392		488			
HC4E35							744	880

[1] WF = Wire bond.
[2] FF = Performance-optimized flip chip.
[3] LF = Cost-optimized flip chip.

636 (8+0) Values on top indicate available user I/O pins; values at the bottom indicate the 6.5-Gbps physical media attachment (PMA) and physical coding sublayer (PCS) plus the 6.5-Gbps PMA-only transceiver count.

All HardCopy series devices are offered in commercial, industrial, and extended temperature grades. Package options include leaded, RoHS-compliant, lidless, or lidded.

	HardCopy III ASICs (0.9 V)					
	FBGA (F)					
	484 (WF) 23 x 23 (mm) 1.0-mm pitch	**484 (FF)** 23 x 23 (mm) 1.0-mm pitch	**780 (WF)** 29 x 29 (mm) 1.0-mm pitch	**780 (FF)** 29 x 29 (mm) 1.0-mm pitch	**1,152 (FF)** 35 x 35 (mm) 1.0-mm pitch	**1,517 (FF)** 40 x 40 (mm) 1.0-mm pitch
HC325	296	296	392	488		
HC335					744	880

636 Number indicates available user I/O pins.

All HardCopy series devices are offered in commercial, industrial, and extended temperature grades. Package options include leaded, RoHS-compliant, lidless, or lidded.

	HardCopy II ASICs (0.9 V)					
	FBGA (F)					
	484 (WF) 23 x 23 (mm) 1.0-mm pitch	**484 (F[1])** 23 x 23 (mm) 1.0-mm pitch	**672 (F)** 27 x 27 (mm) 1.0-mm pitch	**780 (F)** 29 x 29 (mm) 1.0-mm pitch	**1,020 (F)** 33 x 33 (mm) 1.0-mm pitch	**1,508 (F)** 40 x 40 (mm) 1.0-mm pitch
HC210W	308					
HC210		334				
HC220			492	494		
HC230					698	
HC240					742	951

[1] F = Performance-optimized flip chip.

636 Number indicates available user I/O pins.

All HardCopy series devices are offered in commercial, industrial, and extended temperature grades. Package options include leaded, RoHS-compliant, lidless, or lidded.

Arria V GX FPGA Features

		Arria V GX FPGAs (1.1 V)[1], 6.375-Gbps Transceivers							
		5AGXA1	5AGXA3	5AGXA5	5AGXA7	5AGXB1	5AGXB3	5AGXB5	5AGXB7
Density and Speed	ALMs	28,302	56,400	71,698	91,680	113,208	136,880	158,491	190,000
	Equivalent LEs	75,000	149,460	190,000	242,950	300,000	362,730	420,000	503,500
	Registers	113,208	225,555	286,792	366,717	452,830	547,517	633,962	760,000
	M10K memory blocks	800	1,039	1,180	1,366	1,510	1,726	2,054	2,378
	M10K memory (Kb)	8,000	10,390	11,800	13,660	15,100	17,260	20,540	23,780
	MLAB memory (Kb)	463	893	1,173	1,448	1,852	2,098	2,532	2,943
	Variable-precision DSP blocks	240	396	600	800	920	1,045	1,092	1,139
	18-bit x 19-bit multipliers	480	792	1,200	1,600	1,840	2,090	2,184	2,278
	Speed grades: FPGA fabric (fastest to slowest)	-4, -5, -6							
	Speed grades: transceiver (fastest to slowest)	-4, -5, -6							
Architectural Features	Global clock networks	16							
	PLLs/unique outputs	10/40	10/40	12/48	12/48	12/48	12/48	16/64	16/64
	Configuration file size (Mb)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	Design security	✓							
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3[2]							
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)							
	LVDS channels, 1,250 Mbps (receive/transmit)	68	68	120	120	160	160	156	156
	Embedded DPA circuitry	✓							
	Series and differential OCT	✓							
	Programmable drive strength	✓							
	Transceiver (SERDES) channels (6.375 Gbps)	12	12	24	24	24	24	36	36
	PCIe Gen2 x4 hard IP blocks	1	1	2	2	2	2	2	2
	DDR3/2 hard memory controller IP blocks	2	2	4	4	4	4	4	4
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, LPDDR2, SDR							

[1] Maximum LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown.Various packages offer a variety of options to meet your design needs.

[2] 3.3-V compliant, requires a 3-V power supply.

Arria V GT FPGA Features

		Arria V GT FPGAs (1.1 V)[1], Up to 10.3125-Gbps Transceivers	
		5AGTD3	5AGTD7
Density and Speed	ALMs	136,880	190,000
	Equivalent LEs	362,730	503,500
	Registers	547,517	760,000
	M10K memory blocks	1,726	2,378
	M10K memory (Kb)	17,260	23,780
	MLAB memory (Kb)	2,098	2,943
	Variable-precision DSP blocks	1,045	1,139
	18-bit x 19-bit multipliers	2,090	2,278
	Speed grades: FPGA fabric (fastest to slowest)	-5	
	Speed grades: transceiver (fastest to slowest)	-3	
Architectural Features	Global clock networks	16	
	PLLs/unique outputs	12/48	16/64
	Configuration file size (Mb)	TBD	TBD
	Design security	✓	
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3[2]	
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)	
	LVDS channels, 1,250 Mbps (receive/transmit)	120	150
	Embedded DPA circuitry	✓	
	Series and differential OCT	✓	
	Programmable drive strength	✓	
	Transceiver (SERDES) channels (10.3125 Gbps, 6.375 Gbps)	4, 12	8,12
	PCIe Gen2 x4 hard IP blocks	1	1
	DDR3/2 hard memory controller IP blocks	4	4
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, LPDDR2, SDR	

[1] Maximum LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown.Various packages offer a variety of options to meet your design needs.
[2] 3.3-V compliant, requires a 3-V power supply.

Arria V SX SoC FPGA Features

		Arria V SX SoC FPGAs (1.1 V), 6.375-Gbps Transceivers[1]	
		5ASXB3	5ASXB5
Density and Speed	ALMs	132,075	174,340
	Equivalent LEs	350,000	462,000
	Registers	528,300	697,360
	M10K memory blocks	1,729	2,282
	M10K memory (Kb)	17,290	22,820
	MLAB memory (Kb)	2,014	2,658
	Variable-precision DSP blocks	809	1,068
	18-bit x 19-bit multipliers	1,618	2,186
	Speed grades: FPGA fabric (fastest to slowest)	-4, -5, -6	
	Speed grades: transceiver (fastest to slowest)	-4, -5, -6	
Architectural Features	Processor cores (ARM Cortex-A9)	Dual	Dual
	Global clock networks	16	
	FPGA PLLs	10	14
	HPS PLLs	3	3
	Configuration file size (Mb)	TBD	TBD
	Design security	✓	
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3[2]	
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)	
	LVDS channels, 1,250 Mbps (receive/transmit)	120	120
	Embedded DPA circuitry	✓	
	Series and differential OCT	✓	
	Programmable drive strength	✓	
	Transceiver (SERDES) channels (6.375 Gbps)	30	30
	PCIe Gen2 x4 hard IP blocks	2	2
	Maximum FPGA user I/Os	528	528
	Maximum HPS I/Os	216	216
	FPGA hard memory controllers	3	3
	HPS hard memory controllers	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, LPDDR2, SDR	

[1] All data is preliminary.

[2] 3.3-V compliant, requires a 3-V power supply.

Arria V ST SoC FPGA Features

		Arria V ST SoC FPGAs (1.1 V), Up to 10.3125-Gbps Transceivers[1]	
		5ASTD3	5ASTD5
Density and Speed	ALMs	132,075	174,340
	Equivalent LEs	350,000	462,000
	Registers	528,300	697,360
	M10K memory blocks	1,729	2,282
	M10K memory (Kb)	17,290	22,820
	MLAB memory (Kb)	2,014	2,658
	Variable-precision DSP blocks	809	1,068
	18-bit x 19-bit multipliers	1,618	2,186
	Speed grades: FPGA fabric (fastest to slowest)	-5	
	Speed grades: transceiver (fastest to slowest)	-3	
Architectural Features	Processor cores (ARM Cortex-A9)	Dual	Dual
	Global clock networks	16	
	FPGA PLLs	10	14
	HPS PLLs	3	3
	Configuration file size (Mb)	TBD	TBD
	Design security	✓	
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3[2]	
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)	
	LVDS channels, 1,250 Mbps (receive/transmit)	120	120
	Embedded DPA circuitry	✓	
	Series and differential OCT	✓	
	Programmable drive strength	✓	
	Transceiver (SERDES) channels (10.3125 Gbps, 6.375 Gbps)	6, 30	6, 30
	PCIe Gen2 x4 hard IP blocks	2	2
	Maximum FPGA user I/Os	528	528
	Maximum HPS I/Os	216	216
	FPGA hard memory controllers	3	3
	HPS hard memory controllers	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, LPDDR2, SDR	

[1] All data is preliminary.

[2] 3.3-V compliant, requires a 3-V power supply.

Arria II GX FPGA Features

		Arria II GX FPGAs (0.9 V), 6.375-Gbps Transceivers					
		EP2AGX45	EP2AGX65	EP2AGX95	EP2AGX125	EP2AGX190	EP2AGX260
Density and Speed	ALMs	18,050	25,300	37,470	49,640	76,120	102,600
	Equivalent LEs	42,959	60,214	89,178	118,143	181,165	244,188
	Registers[1]	36,100	50,600	74,940	99,280	152,240	205,200
	M9K memory blocks	319	495	612	730	840	950
	MLAB memory (Kb)	564	791	1,171	1,551	2,379	3,206
	Embedded memory (Kb)	2,871	4,455	5,508	6,570	7,560	8,550
	18-bit x 18-bit embedded multipliers	232	312	448	576	656	736
	Speed grades (fastest to slowest)	-3, -4, -5, -6					
Architectural Features	Global clock networks	16					
	Regional clock networks	48					
	Periphery clock networks	50	50	59	59	84	84
	PLLs/unique outputs	4/28	4/28	6/42	6/42	6/42	6/42
	Configuration file size (Mb)	18	18	34	34	64	64
	Design security	✓					
	Others	Plug & Play Signal Integrity					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, BLVDS, Differential SSTL-18, Differential SSTL-15, Differential SSTL-2, Differential HSTL-18, Differential HSTL-12, Differential HSTL-15, SSTL-18 (I and II), SSTL-15 (I), SSTL-2 (I and II), 1.8-V HSTL (I and II), 1.5-V HSTL (I and II), 1.2-V HSTL (I and II)					
	Emulated LVDS channels, 945 Mbps	56	56	64	64	96	96
	LVDS channels, 1,250 Mbps (receive/transmit)	85/84	85/84	105/104	105/104	145/144	145/144
	Embedded DPA circuitry	✓					
	Series and differential OCT	✓					
	Transceiver (SERDES) channels (6.375 Gbps)	8	8	12	12	16	16
	PCIe hard IP block Gen1	1					
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II					

[1] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

Arria II GZ FPGA Features

		Arria II GZ FPGAs (0.9 V), 6.375-Gbps Transceivers		
		EP2AGZ225	EP2AGZ300	EP2AGZ350
Density and Speed	ALMs	89,600	119,200	139,400
	Equivalent LEs	224,000	298,000	348,500
	Registers	179,200	238,400	278,800
	M9K memory blocks	1,235	1,248	1,248
	M144K memory blocks	0	24	36
	MLAB memory (Kb)	2,850	4,420	4,420
	Embedded memory (Kb)	11,100	14,700	16,400
	18-bit x 18-bit embedded multipliers	800	920	1,040
	Speed grades (fastest to slowest)	-3, -4		
Architectural Features	Global clock networks	16		
	Regional clock networks	64	88	88
	Periphery clock networks	88		
	PLLs/unique outputs	8/68	8/96	8/96
	Configuration file size (Mb)	95	141	141
	Design security	✓		
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0		
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15 (I and II), Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), 1.2-V HSTL (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)		
	Emulated LVDS channels, 1,152 Mbps	184	184	184
	LVDS channels, 1,250 Mbps (receive/transmit)	Up to 86		
	Embedded DPA circuitry	✓		
	Series and differential OCT	✓		
	Transceiver (SERDES) channels (6.375 Gbps)	Up to 24		
	PCIe hard IP block (value as 1.1, 2.0, etc)	1		
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR		

Arria Series Package and I/O Matrices

	Arria V GX and GT FPGAs (1.1 V), Up to 10.3125-Gbps Transceivers			
	FBGA (F)			
	672 pin 27 x 27 (mm) 1.0-mm pitch	**896 pin** 31 x 31 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch
5AGXA1	336 9+0	480 12+0		
5AGXA3	336 9+0	480 12+0		
5AGXA5	288 9+0	384 18+0	544 24+0	
5AGXA7	288 9+0	384 18+0	544 24+0	384 18+0
5AGXB1		384 18+0	544 24+0	704 24+0
5AGXB3		384 18+0	544 24+0	704 24+0
5AGXB5			528 24+0	668 36+0
5AGXB7			528 24+0	668 36+0
5AGTD3		322 12+2	544 12+4	704 12+4
5AGTD7			528 12+4	688 12+8

636 / 8+0 Values on top indicate available user I/O pins; values at the bottom indicate the 6.375-Gbps plus 10.3125-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

	Arria V SX and ST SoC FPGAs (1.1 V), Up to 10.3125-Gbps Transceivers[1]		
	FBGA (F)		
	896 pin 31 x 31 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch
5ASXB3	170, 216 12+0	350, 216 18+0	528, 216 30+0
5ASXB5	170, 216 12+0	350, 216 18+0	528, 216 30+0
5ASTD3	170, 216 6+2	350, 216 12+2	528, 216 12+6
5ASTD5	170, 216 6+2	350, 216 12+2	528, 216 12+6

[1] All data is preliminary.

636, 216 / 8+0 Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 6.375-Gbps plus 10.3125-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Arria Series Package and I/O Matrices

	Arria II GX FPGAs (0.9 V), 6.375-Gbps Transceivers			
	UBGA (U)[1]	FBGA (F)		
	358 pin 17 x 17 (mm) 0.8-mm pitch	**572 pin** 25 x 25 (mm) 1.0-mm pitch	**780 pin** 29 x 29 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch
EP2AGX45	156 4	252 8	364 8	
EP2AGX65	156 4	252 8	364 8	
EP2AGX95		260 8	372 12	452 12
EP2AGX125		260 8	372 12	452 12
EP2AGX190			372 12	612 16
EP2AGX260			372 12	612 16

[1]Ultra FineLine ball grid array.

726 / 24 Values on top indicate available user I/O pins; values at the bottom indicate the 6.375-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

	Arria II GZ FPGAs (0.9 V), 6.375-Gbps Transceivers		
	Hybrid FBGA (H)	FBGA (F)	
	780 pin 33 x 33 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch
EP2AGZ225		550 16	726 24
EP2AGZ300	280 16	550 16	726 24
EP2AGZ350	280 16	550 16	726 24

636 / 12 Values on top indicate available user I/O pins; values at the bottom indicate the 6.375-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Cyclone V E FPGA Features

		Cyclone V E FPGAs (1.1 V)				
		5CEA2	5CEA4	5CEA5	5CEA7	5CEA9
Density and Speed	ALMs	9,434	18,113	28,868	56,415	113,585
	Equivalent LEs	25,000	48,000	76,500	149,500	301,000
	Registers	37,736	72,452	115,472	225,660	454,340
	M10K memory blocks	156	312	462	616	1,276
	M10K memory (Kb)	1,560	3,120	4,620	6,160	12,760
	MLAB memory (Kb)	147	283	442	884	1,769
	Variable-precision DSP blocks	39	78	132	220	406
	18-bit x 19-bit multipliers	78	156	264	440	812
	Speed grades: FPGA fabric (fastest to slowest)	-6, -7, -8				
Architectural Features	Global clock networks	16	16	16	16	16
	PLLs/unique outputs	4	4	4	4	4
	Configuration file size (Mb)	TBD	TBD	TBD	TBD	TBD
	Design security	✓				
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HiSpi, SLVS, Sub-LVDS				
	LVDS channels, 875-Mbps receive, 840-Mbps transmit	100	100	100	122	122
	Embedded DPA circuitry	–				
	Series and differential OCT	✓				
	Programmable drive strength	✓				
	PCIe Gen2 x4 hard IP blocks	–				
	DDR3/2 hard memory controller IP blocks	0 or 1	0 or 1	0 or 2	0 or 2	0 or 2
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, LPDDR, LPDDR2				

[1] Maximum LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown.Various packages offer a variety of options to meet your design needs.
[2] 3.3-V compliant, requires a 3-V power supply.

Cyclone V GX FPGA Features

		Cyclone V GX FPGAs (1.1 V), 3.125-Gbps Transceivers				
		5CGXC3	5CGXC4	5CGXC5	5CGXC7	5CGXC9
Density and Speed	ALMs	11,698	18,868	28,868	56,415	113,585
	Equivalent LEs	31,000	50,000	76,500	149,500	301,000
	Registers	46,792	75,472	115,472	225,660	454,340
	M10K memory blocks	120	292	462	616	1,276
	M10K memory (Kb)	1,200	2,920	4,620	6,160	12,760
	MLAB memory (Kb)	147	295	442	884	1,769
	Variable-precision DSP blocks	40	70	132	220	406
	18-bit x 19-bit multipliers	80	140	264	440	812
	Speed grades: FPGA fabric (fastest to slowest)	-6, -7, -8				
	Speed grades: transceiver (fastest to slowest)	-6, -7				
Architectural Features	Global clock networks	16	16	16	16	16
	PLLs/unique outputs	5	6	6	7	8
	Configuration file size (Mb)	TBD	TBD	TBD	TBD	TBD
	Design security	✓				
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HiSpi, SLVS, Sub-LVDS				
	LVDS channels, 875-Mbps receive, 840-Mbps transmit	48	90	100	122	122
	Embedded DPA circuitry	–				
	Series and differential OCT	✓				
	Programmable drive strength	✓				
	Transceiver (SERDES) channels (3.125 Gbps)	3	6	6	9	12
	PCIe Gen2 x4 hard IP blocks	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
	DDR3/2 hard memory controller IP blocks	0 or 1	0 or 2	0 or 2	0 or 2	0 or 2
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, LPDDR, LPDDR2				

[1] Maximum LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown.Various packages offer a variety of options to meet your design needs.
[2] 3.3-V compliant, requires a 3-V power supply.

Cyclone V GT FPGA Features

		Cyclone V GT FPGAs (1.1 V), 5-Gbps Transceivers		
		5CGTD5	5CGTD7	5CGTD9
Density and Speed	ALMs	28,868	56,415	113,585
	Equivalent LEs	76,500	149,500	301,000
	Registers	115,472	225,660	454,340
	M10K memory blocks	462	616	1,276
	M10K memory (Kb)	4,620	6,160	12,760
	MLAB memory (Kb)	442	884	1,769
	Variable-precision DSP blocks	132	220	406
	18-bit x 19-bit multipliers	264	440	812
	Speed grades: FPGA fabric (fastest to slowest)	-6, -7		
	Speed grades: transceiver (fastest to slowest)	-5		
Architectural Features	Global clock networks	16	16	16
	PLLs/unique outputs	6	7	8
	Configuration file size (Mb)	TBD	TBD	TBD
	Design security	✓		
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3		
	I/O standards supported	LLVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HiSpi, SLVS, Sub-LVDS		
	LVDS channels, 875-Mbps receive, 840-Mbps transmit	100	122	122
	Embedded DPA circuitry	–		
	Series and differential OCT	✓		
	Programmable drive strength	✓		
	Transceiver (SERDES) channels (5 Gbps)	6	9	12
	PCIe Gen2 x4 hard IP blocks	2	2	2
	DDR3/2 hard memory controller IP blocks	2	2	2
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, LPDDR, LPDDR2		

[1] Maximum LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown.Various packages offer a variety of options to meet your design needs.
[2] 3.3-V compliant, requires a 3-V power supply.

Cyclone V SE SoC FPGA Features

		Cyclone V SE SoC FPGAs (1.1 V)[1]			
		5CSEA2	5CSEA4	5CSEA5	5CSEA6
Density and Speed	ALMs	9,434	15,094	32,075	41,509
	Equivalent LEs	25,000	40,000	85,000	110,000
	Registers	37,736	60,376	128,300	166,036
	M10K memory blocks	140	224	397	514
	M10K memory (Kb)	1,400	2,240	3,970	5,140
	MLAB memory (Kb)	138	220	480	621
	Variable-precision DSP blocks	36	58	87	112
	18-bit x 19-bit multipliers	72	116	174	224
	Speed grades: FPGA fabric (fastest to slowest)	-6, -7, -8			
Architectural Features	Processor cores (ARM Cortex-A9)	Single or dual	Single or dual	Single or dual	Single or dual
	Global clock networks	16	16	16	16
	FPGA PLLs	4	5	6	6
	HPS PLLs	3	3	3	3
	Configuration file size (Mb)	TBD	TBD	TBD	TBD
	Design security	✓			
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HiSpi, SLVS, Sub-LVDS			
	LVDS channels, 875-Mbps receive, 840-Mbps transmit	31	31	72	72
	Embedded DPA circuitry	–			
	Series and differential OCT	✓			
	Programmable drive strength	✓			
	PCIe Gen2 x4 hard IP blocks	–			
	Maximum FPGA user I/Os	124	124	288	288
	Maximum HPS I/Os	188	188	188	188
	FPGA hard memory controllers	–	1	1	1
	HPS hard memory controllers	1	1	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, LPDDR, LPDDR2			

[1] All data is preliminary.

[2] 3.3-V compliant, requires a 3-V power supply.

Cyclone V SX SoC FPGA Features

		Cyclone V SX SoC FPGAs (1.1 V), 3.125-Gbps Transceivers[1]		
		5CSXC4	5CSXC5	5CSXC6
Density and Speed	ALMs	15,094	32,075	41,509
	Equivalent LEs	40,000	85,000	110,000
	Registers	60,376	128,300	166,036
	M10K memory blocks	224	397	514
	M10K memory (Kb)	2,240	3,970	5,140
	MLAB memory (Kb)	220	480	621
	Variable-precision DSP blocks	58	87	112
	18-bit x 19-bit multipliers	116	174	224
	Speed grades: FPGA fabric (fastest to slowest)	-6, -7, -8		
	Speed grades: transceiver (fastest to slowest)	-6, -7		
Architectural Features	Processor cores (ARM Cortex-A9)	Dual	Dual	Dual
	Global clock networks	16	16	16
	FPGA PLLs	5	6	6
	HPS PLLs	3	3	3
	Configuration file size (Mb)	TBD	TBD	TBD
	Design security	✓		
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3		
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HiSpi, SLVS, Sub-LVDS		
	LVDS channels, 875-Mbps receive, 840-Mbps transmit	31	72	72
	Embedded DPA circuitry	–		
	Series and differential OCT	✓		
	Programmable drive strength	✓		
	Transceiver (SERDES) channels (3.125 Gbps)	6	9	9
	PCIe Gen2 x4 hard IP blocks	2	2	2
	Maximum FPGA user I/Os	124	288	288
	Maximum HPS I/Os	188	188	188
	FPGA hard memory controllers	1	1	1
	HPS hard memory controllers	1	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, LPDDR, LPDDR2		

[1] All data is preliminary.

[2] 3.3-V compliant, requires a 3-V power supply.

Cyclone V ST SoC FPGA Features

		Cyclone V ST SoC FPGAs (1.1 V), 5-Gbps Transceivers[1]	
		5CSTD5	5CSTD6
Density and Speed	ALMs	32,075	41,509
	Equivalent LEs	85,000	110,000
	Registers	128,300	166,036
	M10K memory blocks	397	514
	M10K memory (Kb)	3,970	5,140
	MLAB memory (Kb)	480	621
	Variable-precision DSP blocks	87	112
	18-bit x 19-bit multipliers	174	224
	Speed grades: FPGA fabric (fastest to slowest)	-6, -7	
	Speed grades: transceiver (fastest to slowest)	-5	
Architectural Features	Processor cores (ARM Cortex-A9)	Dual	Dual
	Global clock networks	16	16
	FPGA PLLs	6	6
	HPS PLLs	3	3
	Configuration file size (Mb)	TBD	TBD
	Design security	✓	
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3	
	I/O standards supported	LLVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), HiSpi, SLVS, Sub-LVDS	
	LVDS channels, 875-Mbps receive, 840-Mbps transmit	72	72
	Embedded DPA circuitry	–	
	Series and differential OCT	✓	
	Programmable drive strength	✓	
	Transceiver (SERDES) channels (5 Gbps)	9	9
	PCIe Gen2 x4 hard IP blocks	2	2
	Maximum FPGA user I/Os	288	288
	Maximum HPS I/Os	188	188
	FPGA hard memory controllers	1	1
	HPS hard memory controllers	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, LPDDR, LPDDR2	

[1] All data is preliminary.

[2] 3.3-V compliant, requires a 3-V power supply.

Cyclone IV GX FPGA Features

		Cyclone IV GX FPGAs (1.2 V)[1], Up to 3.125-Gbps Transceivers[2]						
		EP4CGX15	EP4CGX22	EP4CGX30	EP4CGX50	EP4CGX75	EP4CGX110	EP4CGX150
Density and Speed	LEs	14,400	21,280	29,440	49,888	73,920	109,424	149,760
	M9K memory blocks	60	84	120	278	462	666	720
	Embedded memory (Kb)	540	756	1,080	2,502	4,158	5,490	6,480
	18-bit x 18-bit multipliers	0	40	80	140	198	280	360
	Speed grades (fastest to slowest)	-6,-7,-8	-6,-7,-8	-6,-7,-8	-6,-7,-8	-6,-7,-8	-7,-8	-7,-8
Architectural Features	Global clock networks	20	20	20	30	30	30	30
	PLLs/unique outputs	3/15	4/20	4/20	8/40	8/40	8/40	8/40
	Configuration file size (Mb)	3.8	7.6	7.6	24.5	24.5	47.6	47.6
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3						
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)						
	Emulated LVDS channels	9	40	40	73	73	139	139
	LVDS channels, 840 Mbps (receive/transmit)	7/7	14/14	14/14	49/49	49/49	59/59	59/59
	Transceiver (SERDES) channels (2.5 Gbps, 3.125 Gbps)	2, 0	2, 0 / 4, 0	4, 0 / 0, 4[3]	0, 8	0, 8	0, 8	0, 8
	PCIe Gen1 hard IP blocks	1						
External Memory Interfaces	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR						

[1]Maximum LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown. Various packages offer a variety options to meet your design needs.
[2]Transceiver performance varies by product line and package offering.
[3]EP4CGX30 supports 3.125 Gbps only in F484 package option.

Cyclone IV E FPGA Features

		Cyclone IV E FPGAs								
		EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Density and Speed	LEs	6,272	10,320	15,408	22,320	28,848	39,600	55,856	75,408	114,480
	M9K memory blocks	30	46	56	66	66	126	260	305	432
	Embedded memory (Kb)	270	414	504	594	594	1,134	2,340	2,745	3,888
	18-bit x 18-bit multipliers	15	23	56	66	66	116	154	200	266
	Speed grades (fastest to slowest)	-6, -7, -8 -8L, -9L	-6, -7, -8 -8L, -9L	-6, -7, -8 -8L, -9L	-6, -7, -8 -8L, -9L	-6, -7, -8 -8L, -9L	-6, -7, -8 -8L, -9L	-6, -7, -8 -8L, -9L	-6, -7, -8 -8L, -9L	-7, -8 -8L, -9L
Architectural Features	Global clock networks	10	10	20	20	20	20	20	20	20
	PLLs/unique outputs	2/10	2/10	4/20	4/20	4/20	4/20	4/20	4/20	4/20
	Configuration file size (Mb)	2.8	2.8	3.9	5.5	9.1	9.1	14.2	19	27.2
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3								
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2-V HSTL (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II)								
	LVDS channels	66	66	137	52	224	224	160	178	230
External Memory Interfaces	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR								

Cyclone III FPGA Features

		Cyclone III FPGAs (1.2 V)							
		EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
Density and Speed	LEs	5,136	10,320	15,408	24,624	39,600	55,856	81,264	119,088
	M9K memory blocks	46	46	56	66	126	260	305	432
	Embedded memory (Kb)	414	414	504	594	1,134	2,340	2,745	3,888
	18-bit x 18-bit embedded multipliers	23	23	56	66	126	156	244	288
	Speed grades (fastest to slowest)[1]	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-7, -8
Architectural Features	Global clock networks	10	10	20	20	20	20	20	20
	PLLs/unique outputs	2/10	2/10	4/20	4/20	4/20	4/20	4/20	4/20
	Configuration file size (Mb)	2.8	2.8	3.9	5.5	9.1	14.2	19	27.2
	Design security	✓							
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3							
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS							
	Emulated LVDS channels, 840 Mbps	66	66	136	79	223	159	177	229
	Series and differential OCT	✓							
External Memory Interfaces	Memory device supported	QDR II, DDR2, DDR, SDR							

[1]Not all packages are supported in all speed grades.

Cyclone III LS FPGA Features

		Cyclone III LS FPGAs (1.2 V)			
		EP3CLS70	EP3CLS100	EP3CLS150	EP3CLS200
Density and Speed	LEs	70,208	100,488	150,848	198,464
	M9K memory blocks	333	483	666	891
	Embedded memory (Kb)	2,997	4,347	5,994	8,019
	18-bit x 18-bit embedded multipliers	200	276	320	396
	Speed grades (fastest to slowest)[1]	-7, -8			
Architectural Features	Global clock networks	20			
	PLLs/unique outputs	4/20			
	Configuration file size (Mb)	26.8	26.8	50.6	50.6
	Design security	✓			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS			
	LVDS channels, 840 Mbps	169			
	Series and differential OCT	✓			
External Memory Interfaces	Memory device supported	QDR II, DDR2, DDR, SDR			

[1]Not all packages are supported in all speed grades.

Cyclone Series Package and I/O Matrices

	Cyclone V E, GX, and GT FPGAs (1.1 V), Up to 5-Gbps Transceivers						
	UBGA (U)	FBGA (F)					
	484 pin 19 x 19 (mm) 0.8-mm pitch	**256 pin** 17 x 17 (mm) 1.0-mm pitch	**324 pin** 19 x 19 (mm) 1.0-mm pitch	**484 pin** 23 x 23 (mm) 1.0-mm pitch	**672 pin** 25 x 25 (mm) 1.0-mm pitch	**896 pin** 31 x 31 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch
5CEA2	304	144		304			
5CEA4	304	144		304			
5CEA5	240			240	368		
5CEA7	240			240	336	480	
5CEA9					336	448	
5CGXC3	224 3	96 3	112 3	224 3			
5CGXC4	240 6		128 3	240 6	368 6		
5CGXC5	240 6		128 3	240 6	368 6		
5CGXC7	240 6			240 6	336 9	480 9	
5CGXC9						448 12	560 12
5CGTD5	240 6			240 6	368 6		
5CGTD7	240 6			240 6	336 9	480 9	
5CGTD9						448 12	560 12

636 / 12 Values on top indicate available user I/O pins; values at the bottom indicate the 3.125-Gbps or 5-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Cyclone Series Package and I/O Matrices

	Cyclone V SE, SX, and ST SoC FPGAs (1.1 V), Up to 5-Gbps Transceivers[1]		
	UBGA (U)		FBGA (F)
	484 pin 19 x 19 (mm) 0.8-mm pitch	**672 pin** 23 x 23 (mm) 0.8-mm pitch	**896 pin** 31 x 31 (mm) 1.0-mm pitch
5CSEA2	66, 161 0	124, 188 0	
5CSEA4	66, 161 0	124, 188 0	
5CSEA5	66, 161 0	124, 188 0	288, 188 0
5CSEA6	66, 161 0	124, 188 0	288, 188 0
5CSXC4		124, 188 6	
5CSXC5		124, 188 6	288, 188 9
5CSXC6		124, 188 6	288, 188 9
5CSTD5			288, 188 9
5CSTD6			288, 188 9

[1] All data is preliminary.

636, 161 / 12 Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 3.125-Gbps or 5-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Cyclone Series Package and I/O Matrices

	Cyclone IV GX FPGAs (1.2 V), Up to 3.125-Gbps Transceivers					
	QFN (N)[1]	FBGA (F)				
	148 pin 11 x 11 (mm) 0.5-mm pitch	**169 pin** 14 x 14 (mm) 1.0-mm pitch	**324 pin** 19 x 19 (mm) 1.0-mm pitch	**484 pin** 23 x 23 (mm) 1.0-mm pitch	**672 pin** 27 x 27 (mm) 1.0-mm pitch	**896 pin** 31 x 31 (mm) 1.0-mm pitch
EP4CGX15	72 2	72 2				
EP4CGX22		72 2	150 4			
EP4CGX30		72 2	150 4	290 4		
EP4CGX50				290 4	310 8	
EP4CGX75				290 4	310 8	
EP4CGX110				270 4	393 8	475 8
EP4CGX150				270 4	393 8	475 8

[1] Quad flat pack no lead.

636 / 12 — Values on top indicate available user I/O pins; values at the bottom indicate the 2.5-Gbps or 3.125-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

	Cyclone IV E FPGAs (1.0 V and 1.2 V)						
	EQFP (E)[1]	FBGA (F)			MBGA (M)	UBGA (U)	
	144 pin 22 x 22 (mm) 0.5-mm pitch	**256 pin** 17 x 17 (mm) 1.0-mm pitch	**484 pin** 23 x 23 (mm) 1.0-mm pitch	**780 pin** 29 x 29 (mm) 1.0-mm pitch	**164 pin** 8 x 8 (mm) 0.5-mm pitch	**256 pin** 14 x 14 (mm) 0.8-mm pitch	**484 pin** 19 x 19 (mm) 0.8-mm pitch
EP4CE6	91	179				179	
EP4CE10	91	179				179	
EP4CE15	81	165	343		74	165	
EP4CE22	79	153				153	
EP4CE30			328	532			
EP4CE40			328	532			328
EP4CE55			324	374			324
EP4CE75			292	426			292
EP4CE115			280	528			

[1] Enhanced thin quad flat pack.

636 — Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Cyclone Series Package and I/O Matrices

	Cyclone III FPGAs (1.2 V)								
	EQFP (E)	MBGA (M)[1]	PQFP (Q)[2]	FBGA (F)				UBGA (U)	
	144 pin 22 x 22 (mm) 0.5-mm pitch	**164 pin** 8 x 8 (mm) 0.5-mm pitch	**240 pin** 34.6 x 34.6 (mm) 0.5-mm pitch	**256 pin** 17 x 17 (mm) 1.0-mm pitch	**324 pin** 19 x 19 (mm) 1.0-mm pitch	**484 pin** 23 x 23 (mm) 1.0-mm pitch	**780 pin** 29 x 29 (mm) 1.0-mm pitch	**256 pin** 14 x 14 (mm) 0.8-mm pitch	**484 pin** 19 x 19 (mm) 0.8-mm pitch
EP3C5	94	106		182				182	
EP3C10	94	106		182				182	
EP3C16	84	92	160	168		346		168	346
EP3C25	82		148	156	215			156	
EP3C40			128		195	331	535		331
EP3C55						327	377		327
EP3C80						295	429		295
EP3C120						283	531		
EP3CLS70						278	413		278
EP3CLS100						278	413		278
EP3CLS150						210	413		
EP3CLS200						210	413		

[1] Micro FineLine BGA.
[2] Plastic quad flat pack.

636 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

MAX V CPLD Features

		MAX V CPLDs (1.8 V)						
		5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
Density and Speed	LEs	40	80	160	240	570	1270	2210
	Equivalent macrocells[1]	32	64	128	192	440	980	1700
	Pin-to-pin delay (ns)	7.5	7.5	7.5	7.5	9.0	6.2	7.0
	User flash memory (Kb)	8						
	Total on-chip memory (bits)[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Architectural Features	Internal oscillator	✓						
	Digital PLL[3]	✓						
	Fast power on reset	✓						
	Boundary scan JTAG	✓						
	JTAG ISP	✓						
	Fast input registers	✓						
	Programmable register power up	✓						
	JTAG translator	✓						
	Real-time ISP	✓						
I/O Features	MultiVolt I/Os (V)	1.2, 1.5, 1.8, 2.5, 3.3					1.2, 1.5, 1.8, 2.5, 3.3, 5.0[4]	
	I/O power banks	2	2	2	2	2	4	4
	Maximum output enables	54	54	79	114	159	271	271
	LVTTL/LVCMOS	✓						
	LVDS outputs	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	32-bit, 66-MHz PCI compliant	-	-	-	-	-	✓[4]	✓[4]
	Schmitt triggers	✓						
	Programmable slew rate	✓						
	Programmable pull-up resistors	✓						
	Programmable ground pins	✓						
	Open-drain outputs	✓						
	Bus hold	✓						

[1] Typical equivalent macrocells.

[2] Unused LEs can be converted to memory. The total number of available LE RAM bits depends on the memory mode, depth, and width configurations of the instantiated memory.

[3] Optional IP core. Contact your Altera sales representative for availability.

[4] An external resistor must be used for 5-V tolerance.

MAX II CPLD Features

		MAX II CPLDs (3.3 V, 2.5 V, 1.8 V)			
		EPM240/Z	EPM570/Z	EPM1270	EPM2210
Density and Speed	Equivalent macrocells[1]	192	440	980	1,700
	Pin-to-pin delay (ns)	4.7, 7.5	5.4, 9.0	6.2	7.0
Architectural Features	User flash memory (Kb)	8			
	Boundary scan JTAG	✓			
	JTAG ISP	✓			
	Fast input registers	✓			
	Programmable register power up	✓			
	JTAG translator	✓			
	Real-time ISP	✓			
I/O Features	MultiVolt I/Os (V)	1.5, 1.8, 2.5, 3.3	1.5, 1.8, 2.5, 3.3	1.5, 1.8, 2.5, 3.3, 5.0[2]	1.5, 1.8, 2.5, 3.3, 5.0[2]
	I/O power banks	2	2	4	4
	Maximum output enables	80	160	212	272
	LVTTL/LVCMOS	✓			
	32-bit, 66-MHz PCI compliant	-	-	✓[2]	✓[2]
	Schmitt triggers	✓			
	Programmable slew rate	✓			
	Programmable pull-up resistors	✓			
	Programmable ground pins	✓			
	Open-drain outputs	✓			
	Bus hold	✓			

[1] Typical equivalent macrocells.

[2] An external resistor must be used for 5-V tolerance.

MAX 3000A CPLD Features

		MAX 3000A CPLDs (3.3 V)				
		EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A
Density and Speed	Macrocells	32	64	128	256	512
	Equivalent LEs	40	80	160	320	640
	Pin-to-pin delay (ns)	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	7.5, 10	7.5, 10
Architectural Features	Boundary scan JTAG	✓				
	JTAG ISP	✓				
	Fast input registers	✓				
	Programmable register power up	✓				
I/O Features	MultiVolt I/Os (V)	2.5, 3.3, 5.0				
	I/O power banks	1				
	Maximum output enables	6	6	6	6	10
	LVTTL/LVCMOS	✓				
	Programmable slew rate	✓				
	Open-drain outputs	✓				

MAX Series Package and I/O Matrices

MAX V CPLDs (1.8 V)[1]

	EQFP (E)[2]	TQFP (T)[3]		MBGA (M)[4]			FBGA (F)	
	64 pin 7 x 7 (mm) 0.4-mm pitch	100 pin 14 x 14 (mm) 0.5-mm pitch	144 pin 20 x 20 (mm) 0.5-mm pitch	64 pin 4.5 x 4.5 (mm) 0.5-mm pitch	68 pin 5 x 5 (mm) 0.5-mm pitch	100 pin 6 x 6 (mm) 0.5-mm pitch	256 pin 17 x 17 (mm) 1.0-mm pitch	324 pin 19 x 19 (mm) 1.0-mm pitch
5M40Z	54			30				
5M80Z	54	79		30	52			
5M160Z	54	79			52	79		
5M240Z		79	114		52	79		
5M570Z		74	114			74	159	
5M1270Z			114				211	271
5M2210Z							203	271

MAX II CPLDs (3.3 V, 2.5 V, 1.8 V)[1]

	TQFP (T)		FBGA (F)			MBGA (M)			
	100 pin 16 x 16 (mm) 0.5-mm pitch	144 pin 22 x 22 (mm) 0.5-mm pitch	100 pin 11 x 11 (mm) 1.0-mm pitch	256 pin 17 x 17 (mm) 1.0-mm pitch	324 pin 16 x 16 (mm) 0.5-mm pitch	68 pin 5 x 5 (mm) 0.5-mm pitch	100 pin 6 x 6 (mm) 0.5-mm pitch	144 pin 7 x 7 (mm) 0.5-mm pitch	256 pin 11 x 11 (mm) 0.5-mm pitch
EPM240Z						54	80		
EPM570Z							76	116	160
EPM240	80		80				80		
EPM570	76	116	76	160			76		160
EPM1270		116		212					212
EPM2210				204	272				

MAX 3000A CPLDs (3.3 V)

	PLCC (L)[5]	TQFP (T)			PQFP (Q)[6]	FBGA (F)
	44 pin 17.5 x 17.5 (mm) 1.27-mm pitch	44 pin 12 x 12 (mm) 0.5-mm pitch	100 pin 16 x 16 (mm) 0.5-mm pitch	144 pin 22 x 22 (mm) 0.5-mm pitch	208 pin 28 x 28 (mm) 0.5-mm pitch	256 pin 17 x 17 (mm) 1.0-mm pitch
EPM3032A	34	34				
EPM3064A	34	34	66			
EPM3128A			80	96		98
EPM3256A				116	158	161
EPM3512A					172	208

[1] For temperature grades of specific packages (commercial, industrial, or extended temperatures), refer to Altera's online selector guide.
[2] Enhanced quad flat pack.
[3] Thin quad flat pack.
[4] Micro FineLine BGA (0.5 mm).
[5] Plastic J-lead chip carrier.
[6] Plastic quad flat pack.

636 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Quartus II Design Software

www.altera.com/products/software

Quartus II software is number one in performance and productivity for CPLD, FPGA, and ASIC designs, providing the fastest path to convert your concept into reality. Quartus II software also supports many third-party tools in synthesis, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

	Quartus II Design Flow		
	Quartus II Key Features	Availability	
		Subscription Edition	Web Edition (Free)
Design Entry	Cyclone FPGA and MAX CPLD series device support	✓	✓
	Arria and Stratix FPGA series device support	✓	
	HardCopy ASIC device support	✓	
	Multiprocessor support (faster compile time support)	✓	
	IP Base Suite (includes licenses for 15 popular IP cores)	✓	
	Qsys (next-generation system-integration tool)	✓	✓
	SOPC Builder (legacy system development tool)	✓	✓
	Rapid Recompile (faster compile for small design changes)	✓	
	Incremental compile (performance preservation and team-based design)	✓	
Functional Simulation	ModelSim®-Altera Starter Edition	✓	✓
	ModelSim-Altera Edition	✓[1]	✓[1]
Synthesis	Quartus Integrated Synthesis (synthesis tool)	✓	✓
Placement and Routing	Fitter (placement and routing tool)	✓	✓
Timing and Power Verification	TimeQuest tool (static timing analysis)	✓	✓
	PowerPlay tool and optimization (power analysis)	✓	✓
In-System Debug	SignalTap™ II logic analyzer (embedded logic analyzer)[2]	✓	
	Transceiver Toolkit (transceiver interface and verification tool)	✓	
	Operating System Support	Availability	
		Subscription Edition	Web Edition (Free)
	Windows/Linux 32-bit support	✓	✓
	Windows/Linux 64-bit support	✓	

[1] Requires additional license.
[2] Available with talkback feature enabled in Web Edition.

Quartus II Design Software

	Quartus II Design Software Features Summary	
Design Flow Methodology	Incremental compilation[1]	Improves design timing closure and reduces design compilation times up to 70 percent. Supports team-based design.
	Pin planner	Eases the process of assigning and managing pin assignments for high-density and high pin-count designs.
	Qsys (replaces SOPC Builder)	Automates system development by integrating IP functions and subsystems (collection of IP functions) using a hierarchical approach and a high-performance interconnect (based on a network-on-a-chip architecture).
	Off-the-shelf IP cores	Lets you construct your system-level design using IP cores from Altera's megafunction library and from Altera's third-party IP partners.
	Parallel development in ASICs[1]	Allows for FPGA prototypes and HardCopy ASICs to be designed in parallel using the same design software and IP.
	Scripting support	Supports command-line operation and Tcl scripting, as well as GUI design.
	Rapid Recompile[1]	Maximizes your productivity by reducing your compilation time by 50 percent on average (for a small design change after a full compile). Improves design timing preservation.
Performance and Timing Closure Methodology	Physical synthesis	Uses post placement and routing delay knowledge of a design to improve performance.
	Design space explorer (DSE)	Increases performance by automatically iterating through combinations of Quartus II software settings to find optimal results.
	Extensive cross-probing	Provides unmatched support for cross-probing between verification tools and design source files.
	Optimization advisors	Provides design-specific advice to improve performance, resource usage, and power consumption.
	Chip planner	Reduces verification time (while maintaining timing closure) by enabling small, post placement and routing design changes to be implemented in minutes.
Verification	TimeQuest timing analyzer	Provides native Synopsys Design Constraint (SDC) support and allows you to create, manage, and analyze complex timing constraints and quickly perform advanced timing verification.
	SignalTap II embedded logic analyzer	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
	System Console	Enables you to easily debug your FPGA in real time using read and write transactions. It also enables you to quickly create a GUI to help monitor and send data into your FPGA.
	PowerPlay technology	Enables you to accurately analyze and optimize both dynamic and static power consumption.
Third-Party Support	EDA partners	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification. To see a complete list of partners, follow the link: http://www.altera.com/products/software/partners/eda_partners/eda/index.html

[1] Included in Subscription Edition only.

Getting Started Steps

Step 1: Download free Web Edition

http://www.altera.com/support/software/download/sof-download_center.html

Step 2: Get oriented with Quartus II interactive tutorial

After installation, open the interactive tutorial at the welcome screen.

Step 3: Sign up for training

http://www.altera.com/education/training/trn-index.jsp

Quartus II Design Software

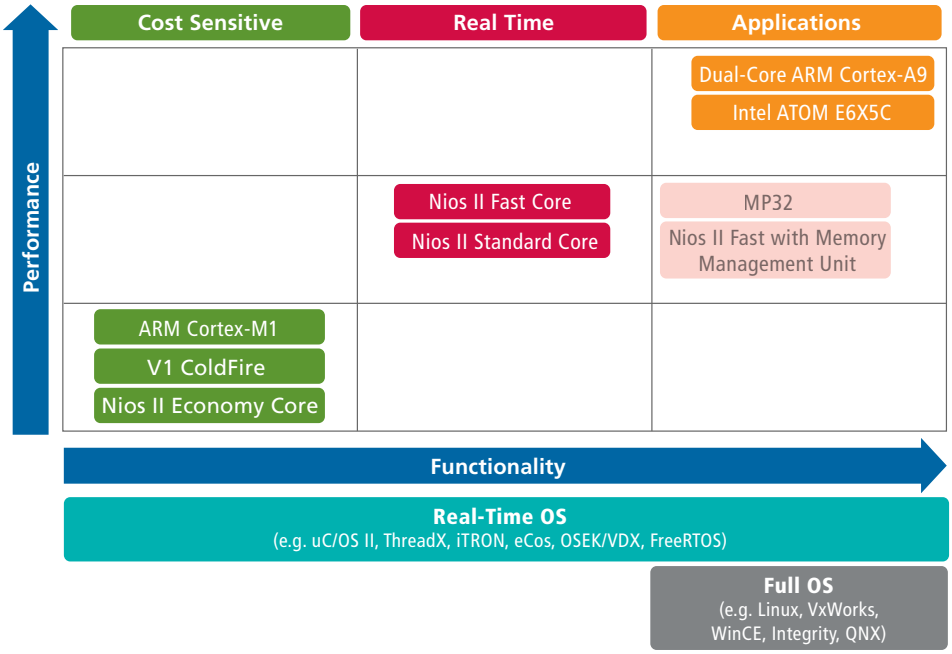
Purchase Quartus II software and increase your productivity today.

Pricing	Description
$2,995 (SW-QUARTUS-SE-FIX) Renewal $2,495 (SWR-QUARTUS-SE-FIX)	Fixed-node license: subscription for one year—Windows only
$3,995 (SW-QUARTUS-SE-FLT) Renewal $2,495 (SWR-QUARTUS-SE-FLT) Add seat $3,995 (SW-QUARTUS-SE-ADD)	Floating-node license: subscription for one year—Windows/Linux

ModelSim-Altera Edition	
$945 (SW-MODELSIM-AE) Renewal $945 (SWR-MODELSIM-AE)	ModelSim-Altera Edition is available as a $945 option for both Quartus II Subscription Edition and Web Edition. It's 33 percent faster than Starter Edition with no line limitation.
ModelSim-Altera Starter Edition	
Free	Free for both Quartus II Subscription Edition and Web Edition with a 10,000 executable line limitation, ModelSim-Altera Starter Edition is recommended for simulating small FPGA designs.

Altera's Customizable Processor Portfolio

Altera's FPGA, SoC FPGA, and HardCopy ASIC devices are increasingly being adopted for custom SoC applications. Altera offers the industry's broadest selection of soft processors, software development tools, OS support, and embedded IP cores. Choose from Altera's customizable processor portfolio to meet your applications, real-time, safety, and power- and cost-sensitive processing needs.



Summary of Processors

Application	Processor	Vendor	Description
Power and cost sensitive	Nios II economy core	Altera	With as low as 600 LEs, the Nios II economy core is ideal for microcontroller applications. The Nios II economy processor, software tools, and device drivers are offered free of charge.
Real time	Nios II standard and fast core	Altera	With unique hardware real-time features such as custom instructions (ability to use FPGA hardware to accelerate a function), vector interrupt controller, tightly coupled memory as well as support for industry-leading real-time OS, the Nios II processor meets both your hard and soft real-time requirements.
Applications processing	Nios II fast core	Altera	A simple configuration option enables the Nios II fast core to use a memory management unit to run embedded Linux. Both open source and commercially support version of Linux for Nios II processors are available.
Applications processing	MP32	SLS	MP32 brings the vast MIPS ecosystem to Altera's FPGAs, such as the VxWorks OS, to enable customizable MIPS-based solutions for video, DSP, and networking.
SoC FPGA	Dual-core ARM Cortex-A9	Altera	Altera's SoC FPGA family integrates an ARM-based HPS, comprising peripherals, memory, and interfaces, with an FPGA fabric.
SoC	Intel® ATOM E6X5C	Intel	The Intel Atom processor E6x5C series provides a customizable Intel Atom processor by combining the Atom processor with an Altera FPGA on a multichip package. It is an ideal platform for netbooks, mobile Internet devices, and automotive infotainment solution development.
Safety critical	Nios II SC	H-Cell	Certify your design for DO-254 compliance by using the Nios II Safety Critical core along with the DO-254 compliance design services offered by H-Cell.
ASIC	Nios II DesignWare IP	Synopsys	Take your embedded design to standard cell ASIC through Synopsys using the Synopsys Nios II DesignWare IP core.

Altera's Customizable Processor Portfolio

Comparative Summary of Altera's Soft Processors by Performance and Feature Set							
Category	**Cost-and Power-Sensitive Processors**			**Real-Time Processor**		**Applications Processors**	
Features	**ARM Cortex-M1**	**V1 ColdFire**	**Nios II Economy**	**Nios II Standard**	**Nios II Fast**	**MP32**	**ARM Cortex-A9**
Maximum frequency (MHz)	200	145	330	270	290	290	800
Maximum performance (MIPS[2] at MHz) Stratix Series	160 at 200	135 at 145	50 at 330	170 at 270	340 at 290	300 at 290	–
Maximum performance (MIPS[2] at MHz) Arria Series	–	84 at 90	45 at 300	115 at 180	270 at 240	300 at 290	2,000 at 800[1]
Maximum performance (MIPS[2] at MHz) Cyclone Series	80 at 100	84 at 90	30 at 175	90 at 145	195 at 175	140 at 145	2,000 at 800[1]
Maximum performance efficiency (MIPS[2] per MHz)	0.8	0.93	0.15	0.64	1.13	1.15	2.5
16-/32-bit instruction set support	16 and 32	16, 32, and 48	32	32	32	32	32
Level 1 instruction cache	–	–	–	Configurable	Configurable	Configurable	32 KB
Level 1 data cache	–	–	–	–	Configurable	64 KB	32 KB
Level 2 cache	–	–	–	–	–	–	512 KB
Memory management unit	–	–	–	–	✓	✓	✓
Floating-point unit	–	–	–	FPCI[3]	FPCI[3]	–	Dual precision
Vector interrupt controller	✓	–	–	✓	✓	–	–
Tightly coupled memory	Up to 64K	–	–	Configurable	Configurable	–	–
Custom instruction interface	–	–	Up to 256	Up to 256	Up to 256	–	–
Equivalent LEs	2,500	6,800	600	1,200	1,800 – 3,200	5,500	HPS

[1] Per processor
[2] Dhrystone 2.1 benchmark
[3] Floating-point custom instructions

Altera's Customizable Processor Portfolio

Available Board Support Package for OS			
Features	**BSP and OS Supplier**	**Nios II Processor**	**MP32**
eCOs	eCosCentric	✓	–
eCos (Zylin)	Zylin	✓	–
embOS	Segger	✓	–
Erika Enterprise	Evidence	✓	–
EUROS RTOS	Euros	✓	–
Linux	Wind River	✓	–
Linux	Timesys	✓	–
Linux	SLS	✓	–
Linux	Open Source	✓	–
MicroC/OS-II	Micrium	✓	–
oSCAN	Vector	✓	–
ThreadX	Express Logic	✓	–
uCLinux	Open Source	✓	–
VxWorks	Wind River	–	✓
RTX RTOS	ARM KEIL	–	–
Toppers RTOS	Open Source	✓	–

Getting Started

Learn more about Altera's portfolio of customizable processors and how you can get started by visiting **www.altera.com/devices/processor/emb-index.html**

Nios II Processor

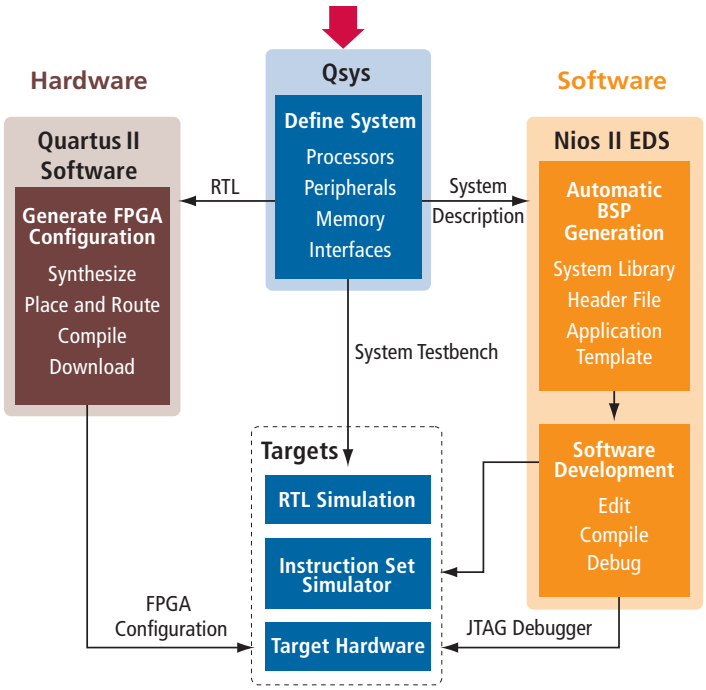
Altera's Nios II processor, the world's most versatile processor according to Gartner Research, is the most widely used soft processor in the FPGA industry. This soft processor delivers unprecedented flexibility for your cost-sensitive, real-time, safety-critical (DO-254), ASIC-optimized, and applications processing needs. The Nios II processor supports all Altera FPGA and HardCopy device families and is also available for standard cell ASICs through Synopsys.

The Nios II processor in any one of Altera's FPGA and HardCopy devices offers a custom SoC solution that has the flexibility of software and the performance of hardware. Through its innovative design, the Nios II processor leverages the logic resources of the device to provide unprecedented hard and soft real-time capabilities.

You can:

- Lower overall system cost, complexity, and power consumption by integrating the processor with the FPGA.
- Scale performance with multiple processors, custom instructions (hardware acceleration of an instruction) or coprocessing (hardware accelerator next to the soft processor).
- Target any Stratix, Arria, or Cyclone series FPGA or HardCopy series ASIC.
- Eliminate the risk of processor and ASSP obsolescence.
- Take advantage of the free Nios II economy core, the free Nios II Embedded Design Suite (EDS), and the NicheStack TCP/IP Network Stack, Nios II Edition software to get started today.

Nios II Processor Development Flow



Nios II EDS Contents
Code Development Tool: Nios II Software Build Tools for Eclipse • New project wizards • Software templates • Source navigator and editor • Compiler for C and C++ (GNU) • Based on industry-standard Eclipse
Source Debugger/Profiler
Flash Programmer
Embedded Software • Hardware Abstration Layer (HAL) • MicroC/OS-II real-time operating system[1] • NicheStack TCP/IP Network Stack—Nios II Edition[1] • Newlib ANSI-C standard library • Simple file system
Other Altera Command-Line Tools and Utilities
Design Examples
C Acceleration Tools: Nios II C-to-Hardware (C2H) Acceleration Compiler[1]

[1] Production license sold separately.

Hardware Development Tools

- Quartus II design software
- Qsys system integration tool
- SignalTap II embedded logic analyzer plug-in for Nios II processor
- System Console for low-level debug of Qsys systems

Licensing

Getting started with the Nios II processor is now easier than ever. Not only is the Nios II EDS free, but the Nios II economy core IP is also free.

As for the Nios II standard and fast core IP, licenses are available as a standalone or as part of the Embedded IP Suite (IPS-EMBEDDED). These royalty-free licenses never expire and allow you to target your processor design on any Altera FPGA. The Embedded IP Suite is a value bundle that contains licenses of the Nios II processor IP core, DDR1/2 Memory Controller IP core, Triple-Speed Ethernet MAC IP core, and the NicheStack TCP/IP Network Stack, Nios II Edition software.

Development Kits

Go to page 59 for information about embedded development kits.

Embedded Design Tool Suite

The Nios II EDS is a collection of all of the tools, utilities, libraries, and drivers needed to develop embedded software for the Nios II processor. It includes the Nios II Software Build Tools for Eclipse for editing, compiling, debugging, and programming flash devices. The Nios II EDS automatically generates a board support package (BSP) for your software application by adding C libraries and device drivers for Altera-provided peripheral IP. The BSP editor provides full control over your build options board support package management.

In addition, the Nios II EDS includes the NicheStack TCP/IP Network Stack, Nios II Edition – a commercial grade network stack software – for free.

Nios II C2H Compiler

Right-click to convert your ANSI-C code into hardware accelerators in the FPGA using the Nios II C2H Acceleration Compiler. Accelerate Nios II embedded software performance from 10X to 70X without increasing clock frequency. The tool automates the creation and integration of hardware accelerators, reducing development time from weeks to minutes.

Altera and Partner Functions

www.altera.com/selector

The following is a partial list of IP functions from Altera and its partners. To get the full story, check out our online selector guide.

	Product Name	Vendor Name
DSP	**Error Detection/Correction**	
	Reed-Solomon Compiler Decoder	Altera
	Reed-Solomon Compiler Encoder	Altera
	Reed-Solomon Encoder/Decoder II[1]	Altera
	Viterbi Compiler, High-Speed Parallel Decoder	Altera
	Viterbi Compiler, Low-Speed/ Hybrid Serial Decoder	Altera
	DVB-RCS CTC Turbo Decoder	TurboConcept
	WiMAX CTC Decoder	TurboConcept
	3GPP/LTE CTC Decoder	TurboConcept
	Turbo Product Code Decoder	TurboConcept
	Filters and Transforms	
	Fast Fourier Transform (FFT)/ Inverse FFT (IFFT)	Altera
	Cascaded Integrator Comb (CIC) Compiler	Altera
	Finite Impulse Response (FIR) Compiler	Altera
	FIR Compiler II	Altera
	2D Forward/Inverse Discrete Cosine Transform	CAST, Inc.
	2D Inverse Discrete Cosine Transform (IDCT)	CAST, Inc.
	Forward Discrete Cosine Transform (DCT)	CAST, Inc.
	Modulation/Demodulation	
	Numerically Controlled Oscillator Compiler	Altera
	DVB-C/J.83 (QAM) Modulator	Commsonic
	DVB/H T/H Modulator	Commsonic
	DVB-S2 Modulator	Commsonic
	Video and Image Processing	
	Video and Image Processing Suite[1]	Altera
	Fast Black and White JPEG Decoder	Barco Silex
	Fast Color JPEG Decoder	Barco Silex
	JPEG2000 Encoder and Decoder	Barco Silex
	JPEG CODEC	CAST, Inc.

	Product Name	Vendor Name
DSP (Continued)	JPEG Encoders and Decoders	CAST, Inc.
	Lossless JPEG Encoder and Decoder	CAST, Inc.
	H.264 AVC High-Definition (HD) Video Encoder	CAST, Inc.
	Color Space Converter	CAST, Inc.
	Forward Discrete Wavelet Transform (FDWT)	Barco Silex
	Inverse Discrete Wavelet Transform (IDWT)	Barco Silex
	V-by-One HS	Bitec
	Display Port Receiver	Bitec
	H.264 Main/ Baseline Profile Encoder	EyeLytics
	Video LVDS SERDES Transmitter/Receiver	Microtronix
	Arithmetic	
	Floating-Point Addition/ Subtraction	Altera
	Floating-Point Multiplication	Altera
	Floating-Point Division	Altera
	Floating-Point Square Root	Altera
	Floating-Point Compare	Altera
	Floating Point Arithmetic Unit	Digital Core Design
	Floating Point Mathematics Unit	Digital Core Design
	Floating Point Pipelined Divider Unit	Digital Core Design
	Floating Point to Integer Pipelined Converter	Digital Core Design
	Integer to Floating Point Pipelined Converter	Digital Core Design
	Additional Functions	
	SHA-1	CAST, Inc.
	SHA-256	CAST, Inc.
	AES CODEC	CAST, Inc.
	AES Programmable Codec	CAST, Inc.
	D/AVE 2D Graphics Hardware Accelerator	TES Electronic Solutions

[1]Qsys-compliant licensed core.

Altera and Partner Functions

	Product Name	Vendor Name
Embedded Processors	**32-/16-Bit**	
	Nios II Embedded Processor[1]	Altera
	ARM Cortex-M1[1]	Arrow Electronics/ARM
	V1 ColdFire[1]	Freescale
	C68000 AHB Microprocessor	CAST, Inc.
	C68000 Microprocessor	CAST, Inc.
	C80186EC Microprocessor	CAST, Inc.
	C80186XL Microprocessor	CAST, Inc.
	8-Bit	
	CZ80CPU Processor	CAST, Inc.
	T8051	CAST, Inc.
	8051XC2 Microcontroller	CAST, Inc.
	DP8051 8-Bit Microcontroller	Digital Core Design
	DP8051XP Pipelined, High Performance 8-Bit Microcontroller	Digital Core Design
	DF6811E 8-Bit Fast Microcontroller	Digital Core Design
	DFPIC1655X 8-Bit RISC Microcontroller	Digital Core Design
Interface and Protocols	**Communication**	
	8B/10B Encoder/Decoder	Altera
	ATM Formatter and Deformatter	Adaptive Micro-Ware, Inc.
	CRC Compiler	Altera
	Frame-Mapped GFP Controller	Nuvation
	GEOS-10: 10:1 Gbps Ethernet to SONET Multiplexer	Nuvation
	GEOS2+2	Nuvation
	POS-PHY Level 4	Altera
	SDLC Controller	CAST, Inc.
	SONET/SDH Deframer	Aliathon

[1]Qsys-compliant licensed core.

	Product Name	Vendor Name
Interface and Protocols (Continued)	SONET/SDH Demapper	Aliathon
	SONET/SDH Framer	Aliathon
	SONET/SDH Mapper	Aliathon
	OTN Framer/Deframer	Altera
	SFI-5.1	Altera
	T1 Framer	Adaptive Micro-Ware, Inc.
	T1 Deframer	Adaptive Micro-Ware, Inc.
	Ethernet	
	10-Gbps Ethernet MAC[1]	Altera
	Tri-Speed Ethernet (MAC and PCS)[1]	Altera
	10G Base-R PHY	Altera
	10G Base-X (XAUI) PHY	Altera
	40G/100G Ethernet	Altera
	40G/100G Ethernet	MorethanIP
	MAC-1G/1G PCS GbE MAC and PCS	CAST, Inc.
	Ethernet MAC Controller with PCI Host Interface (MAC-PCI)	CAST, Inc.
	GbE MAC[1]	IFI
	Advanced GbE MAC[1]	IFI
	EtherCAT (Software Stack)	IXXAT
	Ethernet Powerlink	IXXAT
	EtherNET/IP	IXXAT
	EtherNET/IP	Softing AG
	EtherCAT (Software Stack)	Softing AG
	10/100 Ethernet MAC[1]	SLS Corp
	10GbE MAC and PCS	MorethanIP
	RXAUI PCS	MorethanIP
	SPAUI MAC	MorethanIP

Altera and Partner Functions

Interface and Protocols (Continued)	Product Name	Vendor Name
	10 Gigabit Reduced XAUI PCS	MorethanIP
	Fast XAUI	Octera
	10G MAC Lite	Octera
	High Speed	
	Serial RapidIO®[1]	Altera
	CPRI	Altera
	Interlaken	Altera
	SerialLite II	Altera
	HyperTransport 16-Bit	GDA Technologies
	HyperTransport 3.0	University of Heidelberg
	SATA 1.0/SATA 2.0	Intelliprop, Inc.
	Serial Attached SCSI (SAS) 1.0 and 2.0	Intelliprop, Inc.
	PCI	
	PCIe Gen1 x1[1], x4[1], x8 Controller (Soft IP)	Altera
	PCIe Gen1 and Gen2 x1, x4, and x8 Lane (Hard IP)	Altera
	PCIe Controller	CAST, Inc.
	PCIe x8 Controller	CAST, Inc.
	PCIe Gen1 x1, x4, x8 Controller	Northwest Logic, Inc.
	PCIe Complete Core x1, x4, x8	Northwest Logic, Inc.
	PCIe, Gen1 and Gen2	PLDA
	PCI-X Master/Target Core 32-/64-bit	PLDA
	PCI-X Controller	Northwest Logic, Inc.
	PCI Compiler, 32-Bit Master/Target	Altera
	PCI Compiler, 32-Bit Target	Altera
	PCI Compiler, 64-Bit Master/Target	Altera
	PCI Compiler, 64-Bit Target	Altera
	32-Bit PCI Bus Master/ Target Interface	Eureka Technology, Inc.

Interface and Protocols (Continued)	Product Name	Vendor Name
	32-Bit PCI Host Bridge	Eureka Technology, Inc.
	64-Bit PCI Bus Master/ Target Interface	Eureka Technology, Inc.
	64-Bit PCI Host Bridge	Eureka Technology, Inc.
	Integrated PCI Core	Northwest Logic, Inc.
	PCI Interface	Northwest Logic, Inc.
	PCI 32-/64-Bit PCI Master/ Target 33-/66-MHz Controllers	CAST, Inc.
	PCI Multifunction Target Interface	CAST, Inc.
	PCI Bus Arbiter	Eureka Technology, Inc.
	PCI-ISA Bridge	Eureka Technology, Inc.
	PCI-PCI Bridge	Eureka Technology, Inc.
	Serial	
	I^2C Bus Controller[1]	CAST, Inc.
	I^2C Bus Controller Slave	CAST, Inc.
	DI2CM I^2C Bus Interface-Master	Digital Core Design
	DI2CSB I^2C Bus Interface-Slave	Digital Core Design
	I^2C Master/Slave/PIO Controller	Microtronix, Inc.
	I^2C Master and Slave	SLS
	C_CAN[1]	Bosch
	CAN[1]	CAST, Inc.
	Nios_CAN[1]	IFI
	Nios II Advanced CAN[1]	IFI
	ATA-4 Host Controller	Nuvation
	ATA-5 Host Controller	Nuvation
	MediaLB Device Interface[1]	IFI
	PS2 Interface	SLS
	USB High-Speed Function Controller[1]	SLS
	USB Full/Low-Speed Function Controller[1]	SLS
	CUSB USB Function Controller	CAST, Inc.
	CUSB2 USB High-Speed Function Controller	CAST, Inc.

[1]Qsys-compliant licensed core.

Altera and Partner Functions

	Product Name	Vendor Name
Interface and Protocols (Continued)	USB High-Speed OTG Multi-point	CAST, Inc.
	USB 1.1 Host/Device	Microtronix
	USB 3.0 SuperSpeed[1] Device Controller	PLDA
	USB 3.0 SuperSpeed Device Controller	SLS Corp
	USB 1.1 Host/Device	Microtronix
	SDIO/SD Memory/ Slave Controller	Eureka Technology, Inc.
	AHB Slave	Eureka Technology, Inc.
	AHB Master	Eureka Technology, Inc.
	AHB to SDRAM Controller	Eureka Technology, Inc.
	Local Interconnect Network (LIN) Controller	CAST, Inc.
	SPI Master/Slave	CAST, Inc.
	H16450S UART	CAST, Inc.
	H16550S UART	CAST, Inc.
	D16550 UART with 16-Byte FIFO	Digital Core Design
	H16750S UART	CAST, Inc.
	SPI[1]	Altera
	SPI/Avalon® Master Bridge[1]	Altera
	UART[1]	Altera
	JTAG UART[1]	Altera
	JTAG/Avalon Master Bridge[1]	Altera
	UART	Eureka Technology, Inc.
	MD5	CAST, Inc.
	Smart Card Reader	CAST, Inc.
	DSPI Serial Peripheral Interface Master/Slave	Digital Core Design
	SD Host Controller[2]	SLS

	Product Name	Vendor Name
Interface and Protocols (Continued)	SD/MMC SPI	El Camino GmbH
	SDIO/SD Memory/ MMC Host Controller	Eureka Technology, Inc.
	PowerPC Bus Arbiter	Eureka Technology, Inc.
	PowerPC Bus Master	Eureka Technology, Inc.
	PowerPC Bus Slave	Eureka Technology, Inc.
	AHB to PCI Host Bridge	Eureka Technology, Inc.
	PowerPC/SH/ 1960 System Controller	Eureka Technology, Inc.
	Audio and Video	
	Character LCD[1]	Altera
	Pixel Converter (BGR0 -> BGR)[1]	Altera
	Video Sync Generator[1]	Altera
	ASI	Altera
	SD/HD/3G-HD SDI	Altera
	I2S Audio CODEC[2]	SLS
Memories and Memory Controllers	DMA	
	Scatter Gather DMA Controller[1]	Altera
	DMA Controller[1]	Altera
	DMA for Hard PCIe (EZDMA2)	PLDA
	DMA Controller for AHB[2]	Eureka Technology, Inc.
	Flash	
	NFlashCtrl NAND Flash Memory Controller	CAST, Inc.
	NAND Flash Controller	Eureka Technology, Inc.
	ONFI Controller	Octera
	CompactFlash (True IDE)[1]	Altera
	EPCS Serial Flash Controller[1]	Altera
	Flash Memory[1]	Altera
	CompactFlash Interface[2]	SLS
	ISA/PC Card/PCMCIA/ CompactFlash Host Adapter	Eureka Technology, Inc.

[1]Qsys component (no license required).
[2]Qsys-compliant licensed core.

Altera and Partner Functions

	Product Name	Vendor Name
Memories and Memory Controllers (Continued)	SDRAM	
	Streaming Multi-Port SDRAM Memory Controller	Microtronix
	HyperDrive Multi-Port DDR2 Memory Controller	Microtronix
	DDR and DDR2 SDRAM Controllers[2]	Altera
	DDR and DDR2 SDRAM Controllers supporting ALTMEMPHY[2]	Altera
	DDR2 and DDR3 SDRAM Controllers supporting UniPHY and ALTMEMPHY[2]	Altera
	DDR3 SDRAM Controller supporting ALTMEMPHY[2]	Altera
	DDR SDRAM Controller	CAST, Inc.
	DDR SDRAM Controller	Northwest Logic, Inc.
	DDR2 SDRAM Controller	Northwest Logic, Inc.
	Mobile DDR SDRAM Controller	Northwest Logic, Inc.
	Mobile SDR SDRAM Controller	Northwest Logic, Inc.
	SDR SDRAM[1]	Altera
	SDR SDRAM Controller	CAST, Inc.
	SDR SDRAM Controller	Northwest Logic, Inc.
	Avalon Multi-Port SDRAM Memory Controller[2]	Microtronix
	RLDRAM II Controller supporting UniPHY	Altera
	RLDRAM II Controller	Northwest Logic, Inc.
	SRAM	
	SSRAM (Cypress CY7C1380C)[1]	Altera
	QDR II / II+ Controller supporting UniPHY	Altera
	QDR II SRAM Controller supporting ALTMEMPHY	Altera

[1]Qsys component (no license required).
[2]Qsys-compliant licensed core.

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Altera and Partner Development Kits

The following is a list of Altera and partner development kits. To get the full story, check out our online selector guide.

	Product and Vendor Name	Device	Description
DSP	DSP Development Kit, Cyclone III Edition[1] **Altera**	Cyclone III EP3C120N	This kit is for general DSP or wireless design engineers, regardless of whether you need pre-processing, DSP plus FPGA coprocessing, or post-processsing. This kit includes complete 16-bit high-speed analog-to-digital (A/D) and digital-to-analog (D/A) converters (operating at up to 200 MSPS), as well as interfaces to TI DSP processors (DM642 and DaVinci). Altera's DSP Builder GUI simplifies the information flow between the FPGA toolset and MATLAB/Simulink (30-day evaluation copy included).
	Cyclone III Video and Image Processing Development Kit[1] **Bitec**	Cyclone III EP3C120N	This kit is designed to help you start developing complex video applications. It supports various video I/O interfaces, allowing you to get your video data in and out of the Cyclone III FPGA. Different video interfaces are supported using the different daughtercards included in this kit: cards supporting ASI/SDI, composite, component, and digital video interfaces (DVIs).
	Software Programmable Reconfiguration (SPR) Development System **BittWare**	Cyclone III FPGA	This development system provides a system platform to explore software reconfiguration of waveform functionality for high-end signal processing applications such as software-defined radio. The platform provides a flexible, portable, low-cost environment for software-defined radio development in an Advanced Mezzanine Card (AdvancedMC) and Micro Telecommunications Computing Architecture (MicroTCA) environment, enabling you to quickly and cost-effectively bring your waveform designs to life.
	Audio Video Development Kit, Stratix IV GX Edition **Altera**	Stratix IV GX EP4SGX230	This kit provides a complete video and image processing development environment for design engineers. It features the Stratix IV GX FPGA development board along with an SDI high-speed mezzanine card (HSMC) and associated reference designs.
	DSP Development Kit, Stratix III Edition **Altera**	Stratix III EP3SL150	This kit comprises a Stratix III development board with a HSMC equipped with 16-bit A/D and D/A converters (operating at up to 200 MSPS). The HSMC also has interfaces to TI DSP processors, allowing the designs that use Stratix III FPGAs to be created both as standalone devices and as companion devices. The kit also contains Altera's Quartus II development software, DSP Builder software, and a 30-day trial of MATLAB/Simulink.
	GT-3U-cPCI CompactPCI Board **BittWare**	Stratix II GX EP2SGX90	This is a ruggedized hybrid signal processing board that features a Stratix II FPGA, a TigerSHARC DSP cluster, DDR2 SRAM/QDR SDRAM, flash memory, and an external I/O throughput of 2 Gbps achieved via BittWare's ATLANTiS FrameWork.
	GX-AMC **BittWare**	Stratix II GX FPGA	This is a mid-size, single-width AdvancedMC that can be attached to Advanced Telecommunications Computing Architecture (AdvancedTCA) carriers or other cards equipped with AdvancedMC bays, and used in MicroTCA systems. The GXAM features a high-density Altera Stratix II GX FPGA, BittWare's ATLANTiS FrameWork (implemented in the FPGA), a front panel I/O interface, a control plane interface via BittWare's FINe interface bridge, an IPMI system management interface, and a configurable x8 SERDES interface supporting a variety of protocols. It also provides 10/100 Ethernet, GbE, two banks of DDR2 SDRAM, one bank of QDR II SRAM, and flash memory for booting the FPGA and FINe.

[1] RoHS compliant.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
DSP (Continued)	SC DVI Output Module **Bitec**	Daughtercard	This module supports all Altera development kits with Altera DVI expansion slots.
	THDB-ADA **Terasic Technologies, Inc.**	Daughtercard	This card provides dual A/D channels with 14-bit resolution with data rates up to 65 MSPS and dual D/A channels with 14-bit resolution with data rates up to 125 MSPS. It supports both Altera HSMC and Terasic DE-style connectors.
	HSMC Dual-Link DVI Board **Bitec**	Daughtercard	This is a two-channel, dual-link DVI output board for Altera FPGA development kits with HSMC expansion port.
	SDI HSMC **Terasic Technologies, Inc.**	Daughtercard	This SDI HSMC card is for the development of SDI and AES systems based on transceiver-based host boards with HSMC connectors.
	DE3 Stratix III High Speed Rapid Prototyping System **Terasic Technologies, Inc.**	Stratix III EP3SL150F1152C2N EP3SE260F1152C2N EP3SL340F1152C2N	This board uses the Stratix III devices. Starting with the Stratix III EP3SL150 with 142K LEs, this is the perfect platform for creating your design in programmable logic. DE3 boards are available with either the EP3SL150, the EP3SL340, or the EP3SL260 (DE3-260) devices that are optimized with the extra on-chip multipliers needed for DSP research and development. All of the DE3s can be stacked and all feature the same connector for expanding the base functionality with daughtercards.
	GT-6U-VME **BittWare**	Stratix II GX EP2SGX90FF1508I4	This is a ruggedized 6U VME/VXS (VITA 41) board designed for demanding multiprocessor-based applications. The hybrid processing architecture takes advantage of both FPGA and DSP technology to provide a complete solution for applications requiring flexibility and adaptability along with high-end signal processing. The board features two high-density Stratix II GX FPGAs, a front panel interface supplying four channels of high-speed SERDES tranceivers, and an extensive back panel interface including VXS. The board can achieve simultaneous onboard and offboard data transfers at a rate of 5 Gbps. It also provides up to 3 GB of DDR2 SDRAM, as well as 128 MB of flash memory for booting the FPGAs and DSP devices.
	OmniTek Audio Video **OmniTek**	Arria II GX EP2AGX125EF35	This Arria II GX audio and video development kit combines Altera's proven FPGA-based development hardware and associated IP with OmniTek's expertise in video algorithm IP and PCIe interface design to offer a PCIe Gen1 image processing environment.
	DSP Compute Board **Iris Technologies**	Cyclone II EP2C70	This board features four Cyclone II EP2C70 FPGAs, two DDR2 SODIMMs, and a PCIe x4 Gen1.1 host interface. It is used for Hardware in the Loop (HIL) simulation and emulation, processor and system simulation and emulation, algorithm acceleration, co-processing, and so on. The kit contains drivers, programming cables, Quartus II software, a test design, and C/C++ and MATLAB application programming interfaces (APIs).

[1] RoHS compliant.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
I/O Interconnect	Cyclone IV GX FPGA Development Kit **Altera**	Cyclone IV GX EP4CGX150DF31C7N	This kit provides a comprehensive design environment that allows you to quickly develop low-cost and low-power FPGA system-level designs. This kit includes the PCIe short card form factor, two HSMC connectors, and a 10/100/1000 Mbps Ethernet interface. Onboard memory includes 128-MB DDR2 SDRAM, 64-MB flash, and 4-MB SSRAM. This kit also includes SMA connectors, 50-,100-, and 125-MHz clock oscillators, as well as user interfaces including push buttons, LEDs, and a 7-segment LCD display.
	Arria II GX FPGA Development Kit, 6G Edition **Altera**	Arria II GX EP2AGX125F1152	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to an Arria II GX FPGA up to 6G. This kit includes PCIe x8 form factor, one HSMC connector, 128-MB 16-bit DDR3 device, 1-GB 64-bit DDR2 SODIMM, 2-MB SSRAM, and 64-MB flash.
	Arria II GX FPGA Development Kit **Altera**	Arria II GX EP2AGX125F1152	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to an Arria II GX FPGA. This kit includes PCIe x8 form factor, one HSMC connector, 128-MB 16-bit DDR3 device, 1-GB 64-bit DDR2 SODIMM, 2-MB SSRAM, and 64-MB flash.
	Transceiver Signal Integrity Kit, Stratix IV GX Edition **Altera**	Stratix IV GX EP4SGX230F1517	This kit features eight full-duplex transceiver channels with SMA connectors, 156.25-, 155.52-, 125-, 100-, and 50-MHz clock oscillators, six user push buttons, eight dual in-line package (DIP) switches, eight user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, and Ethernet, USB, and JTAG ports.
	Transceiver Signal Integrity Kit, Stratix V GX Edition **Altera**	Stratix V GX 5SGXEA7N2F40C2NES	This kit enables a thorough evaluation of transceiver signal integrity and device interoperability. Features include seven full-duplex transceiver channels with SMA connectors, two 14G backplane connectors (from Amphenol and Molex), four programmable clock oscillators, four user push buttons, eight DIP switches, eight user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, and Ethernet, embedded USB Blaster™, and JTAG interfaces.
	100G Development Kit, Stratix IV GT Edition **Altera**	Stratix IV GT EP4S100G5F45I1N	This kit enables a thorough evaluation of 100G designs. It supports 10G/40G line interfaces through optical modules, and applications requiring external memory interfaces through four x18 QDR II and four x32 DDR3 memory banks. With this kit, you can evaluate transceiver performance up to 11.3 Gbps, verify PMA compliance to standards such as 10G/40G/100G Ethernet, Interlaken, CEI-6G/11G, Serial RapidIO, PCIe (Gen1, Gen2, and Gen 3), and other major standards, and validate interoperability between optical modules such as SFP, SFP+, QSFP, and CFP.
	Stratix IV GX FPGA Development Kit **Altera**	Stratix IV GX EP4SGX230F1517	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix IV GX FPGA. This kit includes PCIe x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, SDI, and HDMI interfaces. Memory includes one x64 DDR3 SDRAM, one x16 DDR3 SDRAM, two x18 QDR II+ SRAM, flash, and SSRAM. This kit also includes two SMA connectors for a differential transceiver output. Several oscillators are available at 156.25-,155.52-, 125-, 100-, and 50-MHz. Other user interfaces include six user push buttons, eight DIP switches, eight user LEDs, 7-segment LCD display, and power and temperature measurement circuitry.

[1] RoHS compliant.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
I/O Interconnect (Continued)	Stratix IV GX FPGA Development Kit, 530 Edition **Altera**	Stratix IV GX EP4SGX530F1517	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix IV GX FPGA. This kit includes PCIe x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, SDI, and HDMI interfaces. Memory includes one x64 DDR3 SDRAM, one x16 DDR3 SDRAM, two x18 QDR II+ SRAM, flash, and SSRAM. This kit also includes two SMA connectors for a differential transceiver output. Several oscillators are available at 156.25-,155.52-, 125-, 100-, and 50-MHz. Other user interfaces include six user push buttons, eight DIP switches, eight user LEDs, 7-segment LCD display, and power and temperature measurement circuitry.
	Stratix V GX FPGA Development Kit **Altera**	Stratix V GX 5SGXES7K2F40C2N	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix V GX FPGA. This kit includes PCIe x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, and SDI interfaces. Memory includes one x72 DDR3 SDRAM, one x18 QDR II+ SRAM, and flash. This kit also includes two SMA connectors for a differential transceiver output. Several programmable oscillators are available and other user interfaces include three user push buttons, eight DIP switches, eight bi-color user LEDs, an LCD display, and power and temperature measurement circuitry.
	S4GX-AMC **BittWare**	Stratix IV GX EP4SGX230F1517	This board is based on Altera's Stratix IV GX FPGA and is a mid-size, single-width AdvancedMC that can be attached to AdvancedTCA carriers or other cards equipped with AdvancedMC bays, and used in MicroTCA systems. This board has two banks of DDR3 SDRAM (up to 1 GB each), and two banks of QDR II SRAM (up to 9 MB). Includes IP support for Serial RapidIO, PCIe, GbE, 10G Ethernet (XAUI), CPRI, and OBSAI interfaces.
	SF/GX-AMC **BittWare**	Stratix II GX EP2SGX130	This board is based on Altera's Stratix II GX FPGA and is a full-size, single-width AdvancedMC that can be attached to AdvancedTCA carriers or other cards equipped with AdvancedMC bays, and used in MicroTCA systems. The SF/GX-AMC has all the features of the GX-AMC card and includes four small form factor pluggable-plus (SFP/SFP+) compact optical transceiver connectors.
	Ethernet USB Expansion Kit **Microtronix Inc.**	Daughtercard	This kit includes a wireless 802.11b CompactFlash card and a Microtronix CompactFlash board.
	I^2C Design Kit **Microtronix Inc.**	Daughtercard	This kit provides an easy way to design, develop, and test the Microtronix I^2C IP core.
	10/100/1000 Ethernet PHY Daughter Board with Marvell PHY **MorethanIP**	Daughtercard	This kit provides the ability to implement high-speed Ethernet PHY solutions for prototyping and evaluation and embedded software development.
	10/100/1000 Ethernet PHY Daughter Board with National Semiconductor PHY **MorethanIP**	Daughtercard	This kit provides the ability to implement fast Ethernet solutions for prototyping and evaluation and embedded software development.
	SFP HSMC **Terasic Technologies, Inc.**	Daughtercard	This SFP HSMC card is for the development of SGMII Ethernet, Fiber Channel, CPRI/ OBSAI, and SONET designs based on transceiver-based host boards with HSMC connectors.
	Xpress GX4 Kit **PLDA**	Stratix IV GX EP4SGX230KF40C2N	This kit provides a complete hardware and software environment for Altera Stratix IV GX FPGAs. It is built around a PCI form factor card compliant with PCI-SIG® and targets the development of designs using PCIe Gen1 or Gen2.
	PCI-X Development Board **Terasic Technologies, Inc.**	Cyclone III FPGA	This board provides a hardware platform for developing and prototyping low-power, high-performance, logic-intensive PCI-based designs on an Altera Cyclone III FPGA. External memory is provided to facilitate the development of designs that need extra storage capacity or higher bandwidth memory. It also includes a LVDS interface using high-speed Terasic connectors (HSTCs) for high-speed interface applications.
	Xpress AGX2 Kit **PLDA**	Arria II GX EP2AGX125EF35	This kit provides a complete hardware and software environment for Altera Arria II GX FPGAs. It is built around a PCI form factor card compliant with PCI-SIG and targets the development of designs using PCIe Gen1.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
I/O Interconnect (Continued)	Xpress AGX Kit **PLDA**	Arria GX EP1AGX60DF780C6	This kit provides a complete hardware and software environment for Altera Arria GX FPGAs. It is built around a PCI form factor card compliant with PCI-SIG and targets the development of designs using PCIe Gen1.
	Cyclone IV GX Transceiver Starter Kit **Altera**	Cyclone IV GX EP4CGX15	This kit provides a low-cost platform for developing transceiver I/O-based FPGA designs. It includes the complete hardware and software you need to develop your FPGA design for cost-sensitive applications. You can measure the FPGA's power consumption, test the signal quality of the FPGA transceiver I/Os (up to 2.5 Gbps), and develop and test PCIe Gen1 designs.
	Transceiver Signal Integrity Development Kit, Stratix IV GT Edition **Altera**	Stratix IV EP4S100G2F40I1N	This kit enables a thorough evaluation of transceiver interoperability and SERDES signal integrity by allowing you to evaluate transceiver performance up to 11.3 Gbps. You can generate and check pseudo-random binary sequence (PRBS) patterns via a simple-to-use GUI, change differential output voltage (V_{OD}), pre-emphasis, and equalization settings to optimize transceiver performance for your channel, perform jitter analysis, verify PMA compliance to 40G/100G Ethernet, Interlaken, CEI-6G/11G, PCIe (Gen1, Gen2, and Gen3), Serial RapidIO, and other major standards, and validate interoperability between optical modules.
	B2-AMC **BittWare**	Stratix II EP2S90F1020C3	This board supports universal baseband processing for wireless communication infrastructures such as 2G, 2.5G, 3G, WiMAX, and software-defined radio. It attaches to AdvancedTCA carriers or other cards equipped with AdvancedMC bays, and is completely hot-swappable. It uses an Altera Stratix II FPGA, and provides a 10/100/1000 Ethernet interface for command, control, and reprogramming, as well as flash memory for booting the DSP devices and FPGAs.
	Gt-3U-VPX **BittWare**	Stratix II GX EP2SGX90FF1508I4	This is a ruggedized 3U CompactPCI board designed for demanding multiprocessor applications requiring complete flexibility and adaptability. It features an Altera Stratix II GX FPGA, a front panel interface supplying four channels of high-speed SERDES tranceivers, and a back panel interface providing RS-232/RS-422 and 10/100 Ethernet. Simultaneous onboard and offboard data transfers can be achieved at a rate of 2 Gbps. It also provides 1 GB of DDR2 SDRAM and 64 MB of flash memory for booting the FPGA and DSP devices.
	TREX S2 Prototyping System **Terasic Technologies, Inc.**	Stratix II FPGA	This is a Stratix II FPGA prototyping system that provides almost 700 user I/Os and high-speed I/O connections. This board is flexible and configurable, and it provides default motherboards for free—with schematic and design libraries for you to develop your own motherboards.
	QuickUSB Starter Kit **Bitwise Systems**	Cyclone II EP2C20F256C7	This kit includes one QuickUSB module and one QuickUSB Cyclone II Evaluation Board. The evaluation board has a QuickUSB module site on headers that provide access to the signals. The EP2C20F256C7 FPGA connects to nearly every pin of the QuickUSB module, and extra I/O pins go to the headers so you can wire in your circuitry. The kit gets its power from the USB bus, but if you need more power, there is a power connector and a 5V/2A power supply included in the kit.
	C3 Digital Radio Kit **CEPD**	Cyclone III EP3C16	This kit aids the development and testing of algorithms and signal processing applications including digital radio, modulator/demodulator development, software-defined radio, high-speed data acquisition and signal processing, and audio data acquisition and signal processing. The acquired signals are sampled and then digitally processed by a Cyclone III FPGA. The FPGA card comes with a JTAG programming connector and a configuration PROM to retain the FPGA settings. The PCI card provides interfaces for the FPGA card to a computer PCI bus, RS232 interface, and user push buttons and includes a digital radio reference design example and full documentation.
	Cyclone III FPGA/ PCI Development Board **CEPD**	Cyclone III EP3C16F484C8N	This board provides a platform for fast and easy prototyping and design verification with the Cyclone III EP3C16F484C8N FPGA. It can be accessed either through the PCI bus or powered standalone and accessed through an RS232 port. It comes with an onboard configuration PROM to retain the FPGA settings, an RS232 level shifter, voltage monitor, oscillator, buttons, and LEDs. There is a prototyping area on the board for user circuits and all FPGA pins are accessible through connectors and clearly labeled test points. The connectors are designed to mate with other CEPD daughterboards.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
I/O Interconnect (Continued)	XpressGXII Kit **System Level Solutions**	Stratix II GX EP2S- GX130FF1508C3	This kit provides a complete hardware and software environment for Altera Stratix II GX FPGAs. It is built around a PCI form factor card compliant with PCI-SIG and targets the development of designs using PCIe Gen1.
	SuperUSBC3-55 **PLDA**	Cyclone III EP3C55U484C6N	This kit provides a low-cost hardware and software environment for prototyping and deploying SuperSpeed USB applications. It targets the Altera Cyclone III FPGA (EP3C55F484C6N) and includes everything you need to implement a complete USB 3.0 subsystem.
	A01 LVDSS FPGA AMC **Dallas Logic**	Arria GX EP1AGX60	This LVDS transceiver card features the Arria GX FPGA in the F780 BGA package. The backplane interface is user configurable to support several interface standards including PCIe, Serial RapidIO, and GbE. The front panel VHDCI connector supports 28 transmit and 28 receive LVDS links sourced from the FPGA (and 2 clock signals for each transmit and receive connector). Additional features include two 512-Kb x36 synchronous SRAMs, an IPMI 1.5-compliant Module Management Controller (MMC), a 32-Mb serial flash memory, two onboard temperature sensors, USB communication and debug interface, and a 32-bit Mictor debug connector.
	Stratix IV GX/GT 40G/ 100G Interlaken **HiTech Global**	Stratix IV EP4S100G5 EP4SGX530	This board integrates the most fundamental electrical and optical interfaces for building 200G subsystems. It implements CAUI and Interlaken high-speed serial interfaces, industry-leading, high-speed DDR3 and QDR II+ interfaces, and high-speed parallel interconnect for NetLogic knowledge-based processors (KBPs). The modular design enables expansion to support legacy and emerging optical modules.
	HD FIFO Modules **Averlogic**	Daughtercard	This board is designed for evaluating the AL460A HD-FIFO. It has two embedded AL460A-7-PBF (or AL460A-13-PBF) devices operating in parallel, expanding the bus width to 32 bits. Control signals and data bus signals are available on two 50-pin connectors. A separate adaptor board (HSMC interface) is available for connecting the module directly to a Cyclone III FPGA Starter Kit.
	Broadcast Video Card **Bitec**	Daughtercard	This card is designed for professional video equipment developers. The dual ASI/SD-SDI interfaces allow access to industry-standard video transport signals. Based on the latest adaptive cable equalizers and drivers, the ASI/SDI interfaces provide excellent noise immunity up to cable lengths of 350 meters. A VCXO allows precise synchronization to incoming ASI signals. A DVB-T reference design using the Bitec BVDC daughtercard and a Cyclone III FPGA Development Kit is available.
	Quad Video Board **Bitec**	Daughtercard	This board is based on the Texas Instruments TVP5154 quad video decoder. The analog video inputs include composite video and S-video. Video output is based on the Chrontel CH7010B device, enabling single-link DVI, component analog, and composite analog outputs. The device accepts digital, parallel video data, and clocking from the host FPGA via the HSMC connector, which configures and monitors the device over an I^2C link. A DVI output connector and mini-DIN output connector are provided.
	HDMI Receiver/Transmitter **Microtronix**	Daughtercard	This daughtercard interfaces a HDMI receiver and transmitter to your Altera FPGA development kit using the HSMC expansion connector. The receiver also supports an analog component video (YCbCr) interface. The card uses the Analog Device AD9889 HDMI Transmitter and AD9880 HDMI Receiver to support HDTV formats up to 1080p at 60 Hz. The receiver offers the flexibility of both an analog interface and an HDMI receiver integrated on a single chip.
	Quad Link LVDS Interface **Microtronix**	Daughtercard	This daughtercard supports receive and transmit LVDS links, each consisting of five data channels and one clock for a total of 48 LVDS channels. The standard configuration of 20 TX + 4 clk and 20 RX + 2 clk, is capable of supporting LCD display panels up to 1080p at 100/120 Hz. Onboard LVDS termination resistors can be removed to convert receiver channels into transmitters as required to support 12- or 14-bit color applications. It is used for capturing LVDS video data, connecting to a camera link interface, or for connecting to LCD panels using LVDS, mini-LVDS, RSDS, and PPDS low-voltage panel interface signaling.
	CX4 to HSMC Adapter **MorethanIP**	Daughtercard	This is a passive daughtercard for 10GbE CX-4 copper interconnect prototyping. It features a four-lane differential 3.125-Gbps connector (CX-4) for 10GbE IEEE 802.3ak, a 160-pin HSMC to the main board, and compatibility with Stratix II GX mother boards that use HSMC connectors.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
Embedded	Industrial Networking Kit **Terasic Technologies, Inc.**	Cyclone IV E EP4CE115	The Industrial Networking Kit (INK) offers a comprehensive development platform for industrial automation and applications. The kit consists of the DE2-115 board featuring the Altera Cyclone IV device and dual 10/100/1000 Mbps Ethernet, 128-MB SDRAM, 8-MB flash memory, 2-MB SRAM, HSMC and GPIO connectors, USB 2.0, an SD card slot, switches and buttons, LEDs, 16x2 display, audio and video, and VGA-out. The kit also includes an Industrial Communications Board (ICB-HSMC) that supports RS-485, RS-232, CAN, and additional I/O expansion.
	Nios II Embedded Evaluation Kit, Cyclone III Edition[1] **Altera**	Cyclone III EP3C25N	The kit includes a complete hardware and software design environment for a 32-bit microcontroller plus FPGA evaluation. Beginners can check out the pre-built, eye-catching demos displayed on the LCD touch screen or do some lightweight development. Advanced microcontroller designers can learn about the "hottest" techniques, multiprocessor systems, hardware acceleration using Nios II C2H Compiler, or about designing a complete system in 30 minutes.
	Cyclone III FPGA Development Kit **Altera**	Cyclone III EP3C120N	This kit contains 8-MB SSRAM, 256-MB DDR2 SDRAM, 64-MB flash, configuration via USB, 10/100/1000 Ethernet and USB ports, onboard oscillators and SMAs, graphics LCD and character LC displays, two HSMC expansion connectors, three HSMC debug cards, and onboard power measurement circuitry. Complete documentation including reference designs: *Create Your First FPGA Design in an Hour* and *Measure Cyclone III FPGA Power.* This kit also includes Quartus II Web Edition design software, an evaluation edition of Nios II processor plus related design suite, and the Altera IP library.
	Nios II Development Kit, Cyclone III Edition[1] **Altera**	Cyclone III EP3C120N	This development kit has been outfitted with the latest in cutting-edge hardware and software technology. The unique combination of high-performance embedded processor power and easy-to-use integrated design software has been updated to take advantage of Cyclone III devices, the industry's lowest cost, first-to-market 65-nm FPGA family. This development kit provides an ideal environment for developing and prototyping a wide range of price-sensitive, high-performance embedded applications.
	PARIS automotive development platform **TRS-STAR**	Stratix II EP2S90 or EP2S180 Optional path to HardCopy HC210W	This microcontroller development platform creates scalable reference designs for automotive infotainment (head-end, drivers assistance, navigation, and others). Add-on modules and reference designs are also available. Designs can be ported to Altera's automotive-grade Cyclone III FPGAs or HardCopy ASICs.
	Lancelot VGA IP Design Kit **Microtronix Inc.**	Daughtercard	This kit includes a small hardware board with a 24-bit RAMDAC, VGA connector, stereo audio connector, and two PS/2 connectors.
	Compact Flash Expansion Kit **Microtronix Inc.**	Daughtercard	This inexpensive module allows the addition of compact flash cards to the Microtronix Product Starter Kit development board system.
	Low Power Reference Platform **Arrow**	Cyclone III EP3C25 MAX IIG EPM240T100	This platform uses the low-power Altera Cyclone III FPGAs and MAX IIG CPLDs. It demonstrates how to minimize power consumption in portable and battery-powered embedded systems and gives you the flexibility to create application-specific low-power solutions.

[1] RoHS compliant.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
Embedded (Contniued)	MotionFire **Arrow**	Cyclone III EP3C40F484	This kit contains all you need for developing complex motor control applications based on Cyclone III FPGAs. It includes a Nios II reference design, advanced regulators implemented in hardware, generic current, speed, and position regulators with feedback from incremental encoders or hall sensors, a trajectory generator with linear acceleration and velocity feed-forward implemented in software, and much more.
	BeMicro SDK **Arrow**	Cyclone IV E EP4CE22F17C7N	This Arrow BeMicro SDK enables a quick and easy evaluation of soft core processors for both embedded software developers and hardware engineers. The kit builds on the success of the original BeMicro evaluation kit by adding features such as Mobile DDR memory, Ethernet, and even the option of using a file system by slotting in a micro-SD card. The BeMicro SDK connects to a PC via a USB connection, which is used for power, programming, and debug. Arrow has a number of reference designs and pre-built software templates that can be downloaded for this kit that will highlight the benefits of building embedded systems in FPGAs.
	MimoKit **Comsis**	Stratix II EP2S180F1020C5 x2	This kit is designed for extensively networked embedded applications that require wireless LAN connectivity and GbE. It provides the multiple input multiple output (MIMO) RF and analog front end consisting of two major sub-blocks. The analog block is made of three IQ CODECs that perform the conversions between the digital and analog domains. The radio block consists of three 2.4-GHz/5-GHz dual-band radio transceivers.
	ARM-MPS **Gleichmann Electronics**	Stratix III	This platform offers total flexibility for prototyping your ARM Cortex-M3-based designs. It allows unrestricted access to the latest ARM Cortex-M-class processors. It is delivered with a comprehensive range of tools that allow fast and easy system design—drag and drop the supplied IP components to configure the system, or implement your own system blocks. Then synthesize the design and update the board with a single mouse-click. The tool suite also includes system configuration utilities and a JTAG signal monitor together with software development tools and a JTAG debug probe.
	CMCS002M Controller FPGA Module **Dallas Logic**	Cyclone III EP3C25	This module allows you to implement general logic functions and Nios II processor operations in a compact form factor module. The module uses the Cyclone EP3C25 FPGA, 512K x8 SRAM, EP1S16 FPGA serial loader (FPGA and Nios II boot), and a USB 2.0 peripheral port (low-/full-speed operation). This module also supports the Cardstac specification (master or slave standard card, 128 pins), and can interface with other modules designed to that specification.
ASIC Prototyping	DN7020k10 **The Dini Group**	Stratix III Stratix IV	This is a complete logic prototyping system that gives ASIC and IP designers a vehicle to prototype logic and memory designs using up to 20 Stratix III or Stratix IV devices.
	DN7006K10PCIe-8T **The Dini Group**	Stratix III Stratix IV	This is a complete logic prototyping system with a dedicated PCIe interface that gives ASIC and IP designers a vehicle to prototype logic and memory designs using up to six Stratix III or Stratix IV devices.
	DIGILAB SX III **El Camino GmbH**	Stratix III	This is a universal FPGA prototyping platform based on Altera's largest Stratix III devices. Supports 2-MB flash, 2-MB SRAM, four Samtec expansion connectors, two Mictor connectors, user LEDs, and push buttons along with RS-232, SPI, and USB interfaces.
	PROC30M , PROC9M **GiDEL**	Stratix III	This system is for the debug and verification of SoC ASIC designs from 3 to over 100 million gates in size, with the ability to run at system clock speeds up to 300 MHz.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
ASIC Prototyping (Contniued)	PROCStar II, ProcStar III **GiDEL**	Stratix II Stratix III	This system provides high-capacity, high-speed, multi-FPGA-based prototyping and end system platforms.
	DNMEG S2GX Stratix II GX-Based ASIC Prototyping Kit **The Dini Group**	Stratix II GX	This is a logic emulation daughtercard enabling ASIC or IP designers to cost-effectively prototype logic and memory designs. The DNMEG_S2GX is hosted on any DN7000 or DN8000 series ASIC Dini Group product, but can also be used alone.
	S3 Compute **Iris Technologies**	Stratix III Stratix IV	This ASIC prototyping board, compliant with PCI-SIG, features two Altera Stratix III EP3SL340 devices, two DDR2 SODIMM, and four HSMC connectors.
	DN7002k10MEG **The Dini Group**	Stratix IV EP4SE820F43CxN EP4SE530F43CxN	This is a complete logic emulation system that allows you to prototype SoC logic and memory designs. It can operate as a standalone, or hosted via a USB interface. A single system, configured with two Stratix IV EP4SE820 FPGAs, can emulate up to 13 million gates. All FPGA resources are available for the target application. Each FPGA position can use any available speed grade.
	DN7406k10PCIe-8T **The Dini Group**	Stratix IV EP4SE820F43CxN EP4SE530F43CxN	This is a complete logic prototyping system that allows you to prototype logic and memory designs. The DN7406k10PCIe-8T is hosted in an eight-lane PCIe Gen1 bus, but can be used as a standalone and configured via USB or CompactFlash. A single board configured with six Altera Stratix IV EP4SE820 FPGAs can emulate up to 31 million gates. All of the FPGA resources are available for your application. Use any combination of speed grades.
	DNMEG S2GX **The Dini Group**	Stratix II GX EP2SGX90EF1152C3N	This daughtercard enables you to prototype logic and memory designs. It is hosted on any DN8000- or DN7000-series ASIC emulation products from the Dini Group, but can be used as a standalone. It contains the Stratix II GX EP2SGX90 (speed grades -5, -4, or -3) and can emulate over 600K gates. One DDR2 SDRAM SODIMM is provided, allowing the FPGA to address up to 2 GB of memory.
	Stratix IV E FPGA Development Kit **Altera**	Stratix IV E EP4SE530	This kit allows rapid and early development of designs for high-performance Stratix IV FPGAs. The development board provides general I/Os that connect to onboard switches and indicators, and to the included two-line LCD and 128 x 64 graphics display. The board also has non-volatile and volatile memories (64-MB flash, 4-MB pseudo-SRAM, 36-Mb QDR II SRAM, 128-MB DDR2 DIMM, and 16-MB DDR2 device), HSMC, and 10/100/1000 Ethernet interfaces. The kit is delivered with Quartus II software and all of the cabling required to start using the board straight out of the box.
	Stratix III FPGA Development Kit **Altera**	Stratix III EP3SL150	This kit allows rapid and early development of designs for high-performance Stratix III FPGAs. The development board provides general I/Os that connect to onboard switches and indicators, and to the included two-line LCD and 128 x 64 graphics display. The board also has non-volatile and volatile memories (64-MB flash, 4-MB pseudo-SRAM, 36-Mb QDR II SRAM, 128-MB DDR2 DIMM, and 16-MB DDR2 device), HSMC, and 10/100/1000 Ethernet interfaces. The kit is delivered with Quartus II software and all of the cabling required to start using the board straight out of the box.

[1] RoHS compliant.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
General Purpose	Cyclone III FPGA Starter Kit[1] **Altera**	Cyclone III EP3C25N	This kit contains 1-MB SSRAM, 16-MB DDR SDRAM, 16-MB parallel flash, configuration via USB, four user push buttons, four user LEDs, and power measurement circuitry. Complete documentation including reference designs: *Create Your First FPGA Design in a Hour*, *Measure Cyclone III FPGA Power*, and *Create Your First Nios II Design*. This kit also includes Quartus II Web Edition design software, the evaluation edition of Nios II processor plus related design suite, and Altera IP library.
	Video Development Kit **Bitec**	Cyclone III FPGA	This kit contains the Cyclone III FPGA Development Kit and two HSMC video interface cards together with a collection of IP cores and reference designs. The kit provides a variety of video interface standards including both digital and analog up to HD resolutions.
	ViClaro III HD Video Enhancement Development Platform **Microtronix**	Cyclone III FPGA	This is a video enhancement development platform supporting 100/120-Hz HDTV that is 1080p bandwidth-capable and features 32-bit DDR2 SDRAM memory, a HDMI transmitter, an analog/HDMI receiver, and dual LVDS links.
	MAX II Micro **Terasic Technologies, Inc.**	MAX II CPLD	This kit, equipped with an Altera MAX II EPM2210F324C3 device (largest CPLD in the MAX II series) and an onboard USB-Blaster cable, functions as a development and education board for CPLD designs. This kit also includes reference designs with source code.
	DIGILAB picoMAX Prototyping Board and Starter Kit **El Camino GmbH**	MAX EPM3032A to EPM7160S	This is a MAX 3000/MAX 7000 starter kit which includes downloading and programming hardware.
	DB3128 **EBV**	MAX EPM3128A	This is a low-cost MAX 3000A CPLD development board with 128 macrocells that provides an easy entry point into Altera's CPLD technology.
	DB3256 **EBV**	MAX EPM3256A	This is a 5.2-megapixel camera daughtercard with selectable frame rates and resolutions.
	PM410 StarFabric Compact PCI Carrier Board **Parsec**	MAX EPM3256A	This board consists of two 3.3-V PMC sites, 32-/64-bit 33-/66-MHz PCI buses, 2.5-Gbps StarFabric links on J3, and supports full PCI bandwidth.
	TRDB_DC2 1.3 Megapixel Camera Module **Terasic Technologies, Inc.**	Daughtercard	This module consists of complete digital camera reference designs with source code in Verilog HDL and a user manual with live demo examples. It supports exposure, light control, and motion capture.

[1] RoHS compliant.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
General Purpose (Continued)	TRDB_LCM Digital Panel Daughtercard **Terasic Technologies, Inc.**	Daughtercard	This 3.6" digital panel development kit consists of reference designs (TV player and color pattern generator) with source code in Verilog HDL.
	HSMC DVI Input/Output Module **Bitec**	Daughtercard	This DVI transmitter/receiver module for the HSMC interface enables you to interface FPGA projects to real-world DVI signals.
	SC DVI Input Module **Bitec**	Daughtercard	This DVI module for the Santa Cruz interface enables you to interface FPGA projects to real-world DVI signals.
	SC DVI Output Module **Bitec**	Daughtercard	This DVI module for the Santa Cruz interface enables you to drive high-resolution displays with digital clarity.
	SC Camera **Bitec**	Daughtercard	This board features a 5.2-megapixel camera daughtercard with selectable frame rates and resolutions.
	SC Proto **Bitec**	Daughtercard	This is a prototyping board for the Santa Cruz interface with convenient access points to power and ground with connector break-out.
	Hpe-midiv2 **Gleichmann Electronics**	Stratix III EP3SL150	This is a complete development environment with a large number of onboard PHY and a range of child boards with various auxiliary functions for developing large and complex systems. It consists of a motherboard with the latest Stratix III modules and all of the latest interfaces on a single platform. It comes with a graphical user interface for access to a set of free tools including system configuration utilities, JTAG debugger and scanner, and clock factory programmer.
	DE0 Development Board **Terasic Technologies, Inc.**	Cyclone III EP3C16F484C6N	This board provides all the essential tools for you to learn about digital logic and FPGAs. It is equipped with an Altera Cyclone III EP3C16 FPGA, which offers 15,408 LEs. The board provides 346 user I/O pins and is loaded with a rich set of features. It is suitable for advanced university and college courses as well as the development of sophisticated digital systems, and includes software, reference designs, and accessories.
	DE1 Development Board **Terasic Technologies, Inc.**	Cyclone II EP2C20 FPGA	This is a smaller version of the DE2 board. It is useful for learning about digital logic and FPGAs. Featuring an Altera Cyclone II EP2C20 FPGA, it is designed for university and college laboratory use, and is suitable for a wide range of exercises in courses on digital logic and computer organization.
	DE2 Development Board **Terasic Technologies, Inc.**	Cyclone II EP2C35 FPGA	This board was designed by professors, for professors. It is an ideal vehicle for learning about digital logic and FPGAs. Featuring an Altera Cyclone II EP2C35 FPGA, the DE2 board is designed for university and college laboratory use. It is suitable for a wide range of exercises in courses on digital logic and computer organization.
	DE2-70 Digital Camera and Multimedia Development Platform **Terasic Technologies, Inc.**	Cyclone II EP2C70F896C6N	This is a modified version of the Altera DE2 board with a larger FPGA and more memory. It is an excellent vehicle for learning about digital logic and FPGAs. Featuring an Altera Cyclone II EP2C70 FPGA, the DE2 board is designed for university and college laboratory use.
	DE2-115 Development and Education Board **Terasic Technologies, Inc.**	Cyclone IV E EP4CE115	This board is part of the DE2 educational development board series and features the Cyclone IV E EP4CE115 FPGA. The DE2-115 offers an optimal balance of low cost, low power and a rich supply of logic, memory and DSP capabilities, as well as interfaces to support mainstream protocols including GbE. A HSMC connector is provided to support additional functionality and connectivity via HSMC daughtercards and cables.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
General Purpose (Continued)	MAX II/MAX IIZ Development Kit **System Level Solutions**	MAX II EPM240 EPM240Z	This board provides a hardware platform for designing and developing simple and low-end systems based on Altera MAX II/ MAX IIZ devices. The board features a MAX II/MAX IIZ EPM240T100Cx/EPM240ZM100Cx device with 240 LEs and 8,192 bits of user flash memory (UFM). The board also supports vertical migration into EPM570T100Cx devices with 570 LEs and 8,192 bits of UFM.
	MAX V CPLD Development Kit **Altera**	MAX V 5M570Z	This is a low-cost platform to help you quickly begin developing low-cost, low-power CPLD designs. Use this kit as a standalone board or combined with a wide variety of daughtercards that are available from third parties.
	CoreCommander Development Kit **System Level Solutions**	Cyclone III EP3C25F256C8	This kit features the Altera Cyclone III FPGA that provides more than enough room for almost any embedded design. This flexible board comes with a suite of SLS IP Cores, drivers, and application software. Delivered as a complete package, this kit ensures quick and easy implementation of industry-leading cores with reduced risk, at a very low cost.
	Cyclone III LS FPGA Development Kit **Altera**	Cyclone III LS EP3CLS200F780C7N	This kit combines a high-density, low-power Cyclone III LS FPGA with a complete suite of security features implemented at the silicon, software, and IP levels. These security features provide passive and active protection of your IP from tampering, reverse engineering, and counterfeiting. It uses the EP3CLS200 FPGA–200K LEs at less than 1/4 W static power.
	DB Start 3C10 **EBV Elektronik GmbH & Co. KG**	Cyclone III EP3C10E144C8N	This starter kit is ideal for starting your first experiments based on Cyclone III FPGAs. It is designed for ease of use, with embedded USB-Blaster cable and pin header for peripherals. It can be powered via USB, and it features a Linux BSP, a PCI solution for high data throughput, a local bus solution for low-latency data transmission including a local bus IP core, and several industry-standard interfaces such as CAN and RS485.
	DB1270-144 **EBV Elektronik GmbH & Co. KG**	MAX II DB1270T144C5N	This kit enables you to evaluate the MAX II feature set or begin prototyping a design prior to receiving custom hardware. It includes all software, cables, and accessories needed to ensure an easy and productive evaluation of the MAX II CPLD. It includes the MAX II EPM1270T144C5ES CPLD, eight LEDs, four push buttons, a 7-segment display, serial I/O connectors (RS-232 DB9 port), and an 8-bit DIP switch.
	HSMC Prototyping Board **Bitec**	Daughtercard	This board provides a solution for prototyping circuits and testing them together with the latest Altera FPGA development kits. This board provides access to the complete set of HSMC signals via a footprint of standard 0.1" pitch headers. The HSMC power pins are accessed via fuses for added security. The main prototype matrix comprises a 0.1" grid interleaved with +3.3-V and GND access points. Footprints for commonly used 25-way and 9-way D-type connectors are included on the board.

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(All Courses Are One Day in Length Unless Otherwise Noted)

Course Category	General Description	Course Titles
Productivity	Learn the recommended design methodology to maximize productivity and minimize design cycle time	• Best Practices for Maximizing FPGA Design Productivity* (course length: two days)
Design languages	Attain the skills needed to design with Verilog HDL and VHDL for programmable logic	• Introduction to VHDL* • Advanced VHDL Design Techniques* • Introduction to Verilog HDL* • Advanced Verilog HDL Design Techniques*
Software	Acquire design entry, compilation, programming, verification, and optimization skills by learning how to use both basic and advanced features of Quartus II software	• The Quartus II Software Design Series: Foundation* • The Quartus II Software Debug and Analysis Tools • The Quartus II Software Design Series: Timing Analysis* • Advanced Timing Analysis with TimeQuest* • The Quartus II Software Design Series: Optimization*
System integration and embedded design	Build hierarchical systems by integrating IP and custom logic. Learn to design a Nios II soft-core microprocessor system in an Altera FPGA	• System Integration with Qsys (course length: two days) - System Integration with Qsys: Day 1 - System Integration with Qsys: Day 2 • Designing with the Nios II Processor and Qsys (course length: two days) - Designing with the Nios II Processor and Qsys: Day 1 - Designing with the Nios II Processor and Qsys: Day 2 • Developing Software for the Nios II Processor (course length: two days)
Memory interfaces	Implement interfaces to external memory	• Implementing High-Speed Memory Interfaces with Altera FPGAs
DSP and video system design	Solve DSP and video system design challenges using Altera technology	• Designing with DSP Builder Standard Blockset • Designing with DSP Builder Advanced Blockset* • Video System Design with the Video and Imaging Processing Framework
Design security	Create secure, reliable designs using the Quartus II software design separation flow	• Cyclone III LS Design Separation Flow*

Online Training

Altera Free Online Training Courses (Courses Are Approximately One Hour in Length)		
Course Category	Course Titles	Languages
Getting started	Read Me First!	English, Chinese, and Japanese
	Basics of Programmable Logic	English, Chinese, and Japanese
	How to Begin a Simple FPGA Design	English, Chinese, and Japanese
Design languages	VHDL Basics	English and Chinese
	Verilog HDL Basics	English and Chinese
	SystemVerilog with the Quartus II Software	English and Chinese
	Best HDL Design Practices for Timing Closure	English, Chinese, and Japanese
Software overview and design entry	Using Quartus II Software: An Introduction	English, Chinese, and Japanese
	The Quartus II Software Interactive Tutorial	English only
	The Quartus II Software Design Series: Foundation (note: this training is equivalent to the instructor-led course of the same name)	English and Chinese
	What's New in the Quartus II Software Version 11.0	English only
	Setting Up Floating Licenses	English only
	Synplify Pro Tips and Tricks	English only
	Using Quartus II Software: Schematic Design	English and Chinese
	Quartus II Settings and Assignments	Japanese only
	Introduction to Incremental Compilation	English, Chinese, and Japanese
	Team-Based Design Flows Using Quartus II Incremental Compilation	English and Japanese
	I/O System Design	English and Japanese
	Advanced I/O System Design	English and Japanese
	Managing Metastability with the Quartus II Software	English only
Verification and debugging	Overview of Mentor Graphics ModelSim Software	English and Japanese
	Simulating Designs with 3rd Party EDA Simulators	English only
	SignalTap II Embedded Logic Analyzer: Getting Started	English only
	SignTap II Embedded Logic Analyzer	Chinese and Japanese
	Using Quartus II Software: Chip Planner	English only
	Debugging and Communicating with an FPGA Using the Virtual JTAG Megafunction	English only
	System Console Overview	English and Chinese
	Debugging JTAG Chain Integrity	English only

Online Training

Altera Free Online Training Courses (Courses Are Approximately One Hour in Length)		
Course Category	**Course Titles**	**Languages**
Timing analysis and closure	TimeQuest Timing Analyzer	English, Chinese, and Japanese
	Switching to the TimeQuest Timing Analyzer	English and Chinese
	Timing Closure Using Quartus II Advisors and Design Space Explorer	English and Chinese
	Timing Closure Using Quartus II Physical Synthesis Optimizations	English and Chinese
	Timing Closure Using TimeQuest Custom Reporting	English only
Memory interfaces	Using High-Performance Memory Interfaces in Altera FPGAs	English only
	Using UniPHY for High-Speed Memory Interfaces	English and Japanese
	External Memory Solutions Overview	English only
Transceiver-based design and high-speed protocols	Transceiver Basics	English, Chinese, and Japanese
	Transceiver Toolkit	English only
	Decision Feedback Equalization and Adaptive Equalization in Stratix IV GX/GT Devices	English only
	Advanced Signal Conditioning for Stratix IV and Stratix V Receivers	English only
	PCI Express Hard IP Quick Start Guide with SOPC Builder	English, Chinese, and Japanese
	Getting Started with PCI Express Designs in Altera Transceiver Devices	English, Chinese, and Japanese
	PCI Express Compiler Demonstration	English only
	Serial RapidIO Design with Altera 40-nm Devices	English and Chinese
	10/100/1000 Mb Ethernet Design with Altera Transceiver Devices	English and Chinese
	10/100/1000 Mb Ethernet IP Wizard Demonstration	English only
	10Gb Ethernet Design with the Altera MAC MegaCore	English only
	High-Speed Serial Protocol Design with Altera Transceiver Devices	English only
	Stratix V Transceiver Architecture: PMA and PCS Features & Protocol Support	English only
	Stratix V Transceiver Design Flow and Dynamic Reconfiguration	English only
	Dynamic Reconfiguration in Altera Transceiver Devices	English only
	Triple-Rate SDI	English only
DSP and video system design	Designing with DSP Builder Advanced Blockset: An Overview	English and Chinese
	DSP Builder Advanced Blockset Tutorial	Chinese only
	DSP Builder Standard Blockset: An Overview	English only
	Building Video Systems	English and Chinese
	Variable-Precision DSP Blocks in Altera 28-nm FPGAs	English only
	Viterbi Decoder	English only
	Implementing Video Systems	English only
	Using Cascaded-Integrator-Comb Filter in Multirate Digital Systems	English only
	FIR Compiler II	English only

Online Training

Altera Free Online Training Courses (Courses Are Approximately One Hour in Length)		
Course Category	**Course Titles**	**Languages**
Embedded systems	Designing with the Nios II Processor and SOPC Builder (Day 1) (note: this training is equivalent to day 1 of the instructor-led course of the same name)	English only
	Introduction to Qsys	English only
	Advanced System Design Using Qsys	English only
	Developing Software for the Nios II Processor: Tools Overview	English, Chinese, and Japanese
	Developing Software for the Nios II Processor: Design Flow	English and Chinese
	Using SOPC Builder	English and Chinese
	Using the Nios II Processor	English, Chinese, and Japanese
	Nios II Processor and SOPC Builder	Japanese only
	Custom Components for SOPC Builder	English only
	Developing Software for the Nios II Processor: Nios II Software Build Tools for Eclipse	English and Japanese
	Nios II Software Build Tools for Eclipse and BSP Editor (Quartus II Software 10.0 Update)	English only
	Developing Software for the Nios II Processor: Debug Primer	English and Chinese
	Developing Software for the Nios II Processor: HAL Primer	English, Chinese, and Japanese
	Developing Software for the Nios II Processor: Software Build Flow - (Part 1)	English only
	Developing Software for the Nios II Processor: Software Build Flow - (Part 2)	English only
	Developing Software for the Nios II Processor: C2H Fundamentals	English and Japanese
	Nios II Floating-Point Custom Instructions	English and Chinese
	Developing Software for the Nios II Processor: MMU and MPU	English and Chinese
	Avalon Verification Suite	English only
	Lauterbach Debug Tools	English only
	Industrial Ethernet Solutions	English and Chinese
	Introduction to Graphics	English only
	Introduction to D/AVE GPU	English only
Device-specific training	Power Distribution Network Design for Stratix III and Stratix IV FPGAs	English and Chinese
	Power Distribution Network Design Using Altera PDN Design Tools	English only
	Configuring Altera FPGAs	English and Chinese
	The Quartus II Software Design Flow for HardCopy ASICs	English only
Scripting	Command-Line Scripting	English only
	Introduction to Tcl Part 1 of 2	English only
	Introduction to Tcl Part 2 of 2	English only
	Basic Quartus II Software Tcl Scripting Part 1 of 2	English and Japanese
	Basic Quartus II Software Tcl Scripting Part 2 of 2	English only

Protocols, Devices, and Data Rates

Protocols, Devices, and Data Rates						
Protocol	**Stratix V GX/GS Data Rates (Gbps per Lane)**	**Stratix V GT Data Rates (Gbps per Lane)**	**Stratix IV GX Data Rates (Gbps per Lane)**	**Stratix IV GT Data Rates (Gbps per Lane)**	**Stratix II GX Data Rates (Gbps per Lane)**	**HardCopy IV GX Data Rates (Gbps per Lane)**
3G-SDI	2.97	2.97	2.97	2.97	2.97	2.97
SDI SD/HD	0.27 / 1.485	0.27 / 1.485	0.27 / 1.485	0.2 / 1.485	0.27 / 1.485	0.27 / 1.485
ASI	0.27	0.27	0.27	0.27	0.27	0.27
Basic (proprietary)	0.6 – 14.1	0.6 – 12.5, 19.6 – 28.05	0.6 – 8.5	0.6 – 11.3	0.6 – 6.375	0.6 – 6.5
CEI-6G/SR/LR	4.976 – 6.375	4.976 – 6.375	4.976 – 6.375	4.976 – 6.375	4.976 – 6.375	4.976 – 6.375
CEI-11G/SR	9.95 – 11.1	9.95 – 11.1	-	9.95 – 11.1	-	-
CEI-28G/VSR	-	19.9 – 28.05	-	-	-	-
CPRI	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144, 9.8304	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144, 9.8304	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144	0.6144, 1.2288, 2.4576, 3.072
Display Port	-	-	-	-	-	-
10G Ethernet (XAUI)	3.125	3.125	3.125	3.125	3.125	3.125
10G Ethernet (XFI)	10.3125	10.3125	-	10.3125	-	-
40G/100G Ethernet	10.3125	10.3125	-	10.3125	-	-
GbE	1.25	1.25	1.25	1.25	1.25	1.25
Fibre Channel	1.0625, 2.125, 4.25, 8.5, 10.52, 14.025	1.0625, 2.125, 4.25, 8.5, 10.52, 14.025	1.0625, 2.125, 4.25, 8.5	1.0625, 2.125, 4.25, 8.5, 10.52	1.0625, 2.125, 4.25	1.0625, 2.125, 4.25
GPON	1.244 uplink/ 2.488 downlink, 2.488 uplink/ 9.953 downlink	1.244 uplink/ 2.488 downlink, 2.488 uplink/ 9.953 downlink	1.244 uplink, 2.488 downlink	1.244 uplink, 2.488 downlink	-	1.244 uplink, 2.488 downlink
G.709 OTU-2	10.7	10.7	-	10.7	-	-
OTN, 10GbE with FEC	11.1, 11.3	11.1, 11.3	-	11.1, 11.3	-	-
HiGig+	3.75	3.75	3.75	3.75	3.75	3.75
HiGig2	4.0625	4.0625	4.0625	4.0625	4.0625	4.0625

Protocols, Devices, and Data Rates

Protocols, Devices, and Data Rates						
Protocol	**Arria V GX Data Rates (Gbps per Lane)**	**Arria V GT Data Rates (Gbps per Lane)**	**Arria II GX/GZ Data Rates (Gbps per Lane)**	**Cyclone V GX Data Rates (Gbps per Lane)**	**Cyclone V GT Data Rates (Gbps per Lane)**	**Cyclone IV GX Data Rates (Gbps per Lane)**
3G-SDI	2.97	2.97	2.97	2.97	2.97	2.97
SDI SD/HD	0.27 / 1.485	0.27 / 1.485	0.27 / 1.485	0.27 / 1.485	0.27 / 1.485	0.27 / 1.485
ASI	-	-	0.27	-	-	-
Basic (proprietary)	0.6 – 6.5	0.6 – 10.3125	0.6 – 6.375	0.6 – 3.125	0.6 – 5.0	0.6 – 3.125
CEI-6G/SR/LR	4.976 – 6.375	4.976 – 6.375	-	-	-	-
CPRI	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144,	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144, 9.8304	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144	0.6144, 1.2288, 2.4576, 3.072	0.6144, 1.2288, 2.4576, 3.072, 4.915	0.6144, 1.2288, 2.4576, 3.072
Display Port	1.62, 2.7	1.62, 2.7	-	1.62, 2.7	1.62, 2.7	1.62, 2.7
10G Ethernet (XAUI)	3.125	3.125	3.125	3.125	3.125	3.125
10G Ethernet (XFI)	-	10.3125	-	-	-	-
40G/100G Ethernet	-	-	-	-	-	-
GbE	1.25	1.25	1.25	1.25	1.25	1.25
Fibre Channel	-	-	1.0625, 2.125, 4.25	-	-	-
GPON	1.244 uplink, 2.488 downlink	1.244 uplink, 2.488 downlink	1.244 uplink, 2.488 downlink	-	-	-
G.709 OTU-2	-	-	-	-	-	-
OTN, 10GbE with FEC	-	-	-	-	-	-
HiGig+	3.75	3.75	3.75	-	-	-
HiGig2	4.0625	4.0625	-	-	-	-

Protocols, Devices, and Data Rates

Protocols, Devices, and Data Rates						
Protocol	**Stratix V GX/GS Data Rates (Gbps per Lane)**	**Stratix V GT Data Rates (Gbps per Lane)**	**Stratix IV GX Data Rates (Gbps per Lane)**	**Stratix IV GT Data Rates (Gbps per Lane)**	**Stratix II GX Data Rates (Gbps per Lane)**	**HardCopy IV GX Data Rates (Gbps per Lane)**
HyperTransport 3.0	0.4, 2.4, 2.8, 3.2	0.4, 2.4, 2.8, 3.2	0.4, 2.4, 2.8, 3.2	0.4, 2.4, 2.8, 3.2	-	0.4, 2.4, 2.8, 3.2
IEEE 802.3ba 10GBASE-KR	10.3125	10.3125	-	-	-	-
Interlaken	3.125 – 12.5	3.125 – 12.5	3.125 – 8.5	3.125 – 11.3	3.125 – 6.375	3.125 – 6.375
OBSAI	0.768, 1.536, 3.072, 6.144	0.768, 1.536, 3.072, 6.144	0.768, 1.536, 3.072	0.768, 1.536, 3.072, 6.144	0.768, 1.536, 3.072, 6.144	0.768, 1.536, 3.072, 6.144
PCIe Gen1, Gen2, Gen3	2.5, 5, 8	2.5, 5, 8	2.5, 5, N/A	2.5, 5, N/A	2.5, 5, N/A	2.5, 5, N/A
PCIe Cable	2.5	2.5	2.5	2.5	2.5	2.5
RXAUI	6.25	6.25	6.25	6.25	6.25	6.25
QDR Infiniband	10.0	10.0	-	-	-	-
QPI	6.4	6.4	-	-	-	-
SAS	1.5, 3, 6	1.5, 3, 6	1.5, 3, 6	1.5, 3, 6	-	1.5, 3, 6
SAS 12G	1.5, 3, 6, 12	1.5, 3, 6, 12	-	-	-	-
SATA	1.5, 3, 6	1.5, 3, 6	1.5, 3, 6	1.5, 3, 6	-	1.5, 3, 6
SerialLite II	0.6 – 6.375	0.6 – 6.375	0.6 – 6.375	0.6 – 6.375	0.6 – 6.375	0.6 – 6.375
Serial RapidIO	1.25, 2.5, 3.125, 5.0, 6.25	1.25, 2.5, 3.125, 5.0, 6.25	1.25, 2.5, 3.125, 5.0, 6.25	1.25, 2.5, 3.125, 5.0, 6.25	1.25, 2.5, 3.125	1.25, 2.5, 3.125
SFI-5.1	2.488 – 3.125	2.488 – 3.125	2.488 – 3.125	2.488 – 3.125	2.488 – 3.125	2.488 – 3.125
SFI-5.2	9.9 – 11.3	9.9 – 11.3	-	9.9 – 11.3	-	-
SONET OC-3/OC-12/ OC-48/OC-192	0.155, 0.622, 2.488, 9.953	0.155, 0.622, 2.488, 9.953	0.155, 0.622, 2.488, N/A	0.155, 0.622, 2.488, 9.953	0.155, 0.622, 2.488, N/A	0.155, 0.622, 2.488, N/A
SPAUI	3.125, 6.25	3.125, 6.25	3.125, 6.25	3.125, 6.25	3.125, 6.25	3.125, 6.25
V-by-One	-	-	-	-	-	-

Protocols, Devices, and Data Rates

Protocols, Devices, and Data Rates						
Protocol	**Arria V GX Data Rates (Gbps per Lane)**	**Arria V GT Data Rates (Gbps per Lane)**	**Arria II GX/GT Data Rates (Gbps per Lane)**	**Cyclone V GX Data Rates (Gbps per Lane)**	**Cyclone V GT Data Rates (Gbps per Lane)**	**Cyclone IV GX Data Rates (Gbps per Lane)**
HyperTransport 3.0	0.4, 2.4, 2.8, 3.2	0.4, 2.4, 2.8, 3.2	-	-	-	-
IEEE 802.3ba 10GBASE-KR	-	-	-	-	-	-
Interlaken	3.125 – 6.375	3.125 – 6.375	-	-	-	-
OBSAI	0.768, 1.536, 3.072, 6.144	0.768, 1.536, 3.072, 6.144	0.768, 1.536, 3.072, 6.144	0.768, 1.536, 3.072	0.768, 1.536, 3.072	0.768, 1.536, 3.072
PCIe Gen1, Gen2, Gen3	2.5, 5, N/A	2.5, 5, N/A	2.5, 5.0, N/A	2.5, N/A, N/A	2.5, 5.0, N/A	2.5, N/A, N/A
PCIe Cable	2.5	2.5	2.5	2.5	2.5	2.5
RXAUI	6.25	6.25	-	-	-	-
QDR Infiniband	-	-	-	-	-	-
QPI	-	-	-	-	-	-
SAS	1.5, 3.0, 6.0	1.5, 3.0, 6.0	1.5, 3.0, 6.0	-	-	-
SATA	1.5, 3.0, 6.0	1.5, 3.0, 6.0	1.5, 3.0, 6.0	1.5, 3.0	1.5, 3.0	1.5, 3.0
SerialLite II	-	-	0.6 – 3.75	-	-	-
Serial RapidIO	1.25, 2.5, 3.125, 5.0, 6.25	1.25, 2.5, 3.125, 5.0, 6.25	1.25, 2.5, 3.125	1.25, 2.5, 3.125	1.25, 2.5, 3.125	1.25, 2.5, 3.125
SFI-5.1	2.488 – 3.125	2.488 – 3.125	-	-	-	-
SFI-5.2	-	-	-	-	-	-
SONET OC-3/OC-12/ OC-48/OC-192	0.155, 0.622, 2.488, N/A	0.155, 0.622, 2.488, N/A	0.155, 0.622, 2.488, N/A	-	-	-
SPAUI	-	-	3.125	-	-	-
V-by-One	3.75	3.75	-	3	3.75	3.0

Configuration Devices

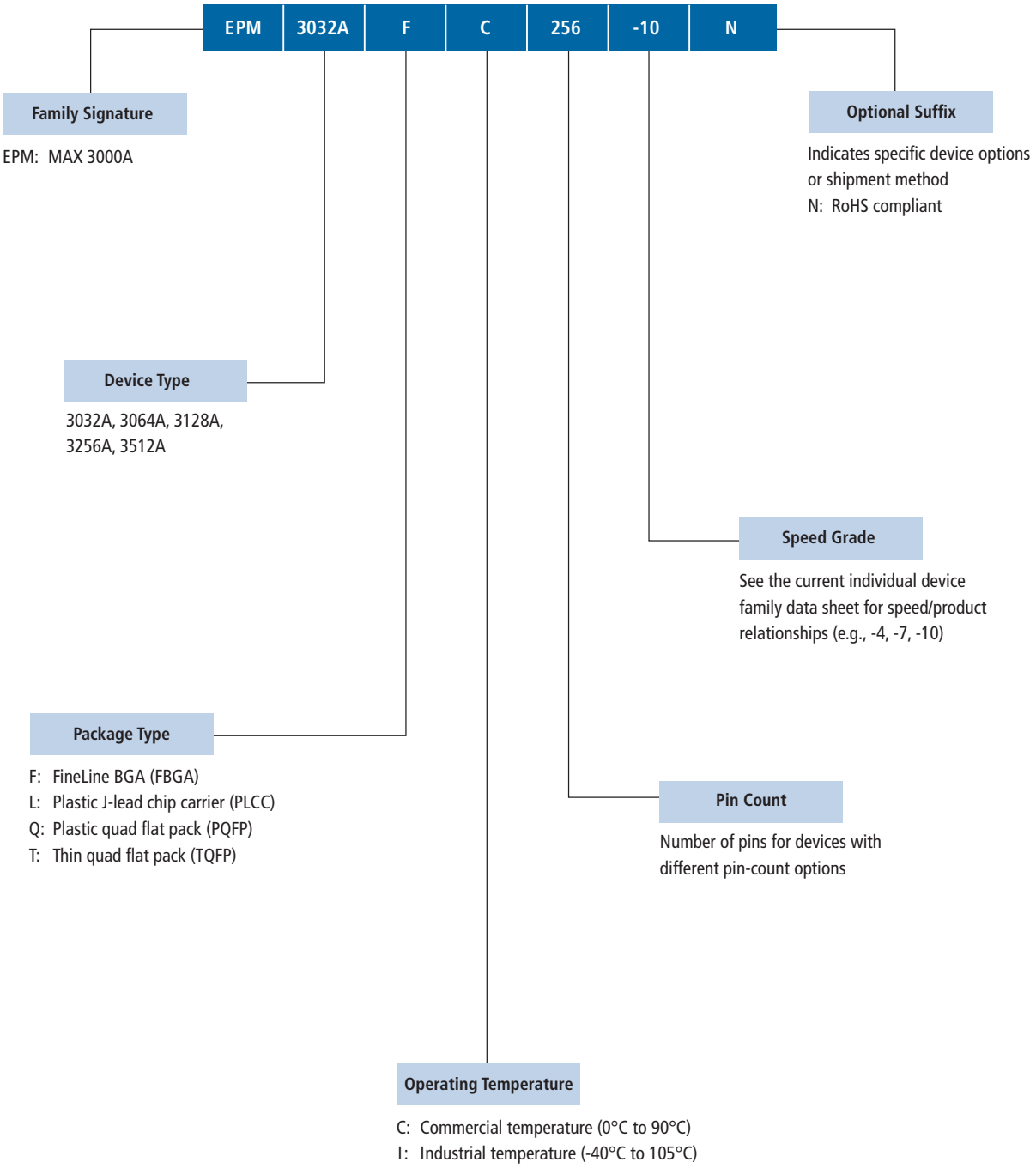
www.altera.com/literature/lit-config.jsp

The following is an overview of our configuration devices. To determine the right configuration device for your FPGA, check out our Configuration Handbook or the configuration chapter in the handbook of your selected FPGA.

Altera's serial configuration devices store the configuration file for our SRAM-based FPGAs. We designed our serial configuration devices to minimize cost and board space while providing a dedicated FPGA configuration solution. Serial configuration devices are recommended for new designs. For information on additional configuration devices supporting older products, see our Configuration Handbook.

Serial Configuration Device	Memory Size (Bits)	Package
EPCS1	1,048,576	SOIC8
EPCS4	4,194,304	SOIC8
EPCS16	16,777,216	SOIC8
EPCS64	67,108,864	SOIC16
EPCS128	134,217,728	SOIC16

Ordering Codes



Ordering Codes

EP1S	25	F	780	C	5	N

Family Signature

5M: MAX V
EPM: MAX II
EP4CE: Cyclone IV E
EP4CGX: Cyclone IV GX
EP3CLS: Cyclone III LS
EP3C: Cyclone III
EP2C: Cyclone II
EP1C: Cyclone
EP2AGZ: Arria II GZ
EP2AGX: Arria II GX
EP1AGX: Arria GX
EP4SE: Stratix IV E
EP4SGX: Stratix IV GX
EP4S: Stratix IV GT
EP3SL: Stratix III L
EP3SE: Stratix III E
EP2S: Stratix II
EP2SGX: Stratix II GX
EP1S: Stratix
EP1SGX: Stratix GX
HC4E: HardCopy IV E
HC4GX: HardCopy IV GX
HC3: HardCopy III
HC2: HardCopy II

Device Type

5M: 40, 80, 160, 240, 570, 1270, 2210
EPM: 240, 570,1270, 2210
EP4CE: 6, 10, 15, 30, 40, 55, 75, 115
EP4CGX: 15, 22, 30, 50, 75, 110, 150
EP3CLS: 70, 100, 150, 200
EP3C: 5, 10, 16, 25, 40, 55, 80, 120
EP2C: 5, 8, 8A, 15A, 20, 20A, 35, 50, 70
EP1C: 3, 4, 6,12, 20
EP2AGZ: 225, 300, 350
EP2AGX: 20, 30, 45, 65, 95, 125, 190, 260
EP1AGX: 20, 35, 50, 60, 90
EP4SE: 110, 230, 290, 360, 530, 680
EP4SGX: 70, 110, 230, 290, 360, 530
EP4S: 40G, 100G
EP3SL: 50, 70, 110, 150, 200, 340
EP3SE: 50, 80, 110, 260
EP2S: 15, 30, 60, 90, 130,180
EP2SGX: 30, 60, 90, 130
EP1S: 10, 20, 25, 30, 40, 60, 80
EP1SGX: 10, 25, 40
HC4E: 25, 35
HC4GX: 15, 25, 35
HC3: 25, 35
HC2: 10W, 10, 20, 30, 40

Transceiver Channels

For transceiver-based FPGAs (GX/GZ/GT) only

C: 4
D: 8
E: 12
F: 16
G: 20
H: 24
K: 36
N: 48

Package Type

B: Ball-grid array
E: Enhanced thin quad flat pack
F: FineLine BGA
H: Hybrid FineLine BGA
M: Micro BGA
Q: Plastic quad flat pack
T: Thin quad flat pack
U: Ultra FineLine BGA

Pin Count

Number of pins for devices with different pin-count options

Note: Stratix IV E, Stratix IV GX, Stratix IV GT, and Arria II GX devices use package size in place of pin counts:

Package type/size:	Package type/pin count:
F29/H29	F780/H780
F35/H35	F1152/H1152
F40/H40	F1517/H1517
F43	F1760
F45	F1932

Product-Line Suffix

For MAX II devices only
Indicates device core voltage
G: 1.8V V_{CCINT} device
Blank: 2.5V or 3.3V V_{CCINT} device
Z: zero power device

Operating Temperature

A: Automotive grade (-40°C to 125°C)
C: Commercial temperature (0°C to 85°C)
I: Industrial temperature (-40°C to 100°C)
M: Military temperature (-55°C to 125°C)

Speed Grade

Devices	Fast ← 1	2	3	4	5	6	7	8 → Slow
MAX V				✓	✓			
MAX II			✓	✓	✓			
Cyclone IV E						✓	✓	✓
Cyclone IV GX						✓	✓	✓
Cyclone III LS							✓	✓
Cyclone III						✓	✓	✓
Cyclone II						✓	✓	✓
Cyclone						✓	✓	✓
Arria II GZ			✓	✓				
Arria II GX			✓	✓	✓	✓		
Arria GX						✓		
Stratix IV E		✓	✓	✓				
Stratix IV GX		✓	✓	✓				
Stratix IV GT	✓	✓	✓					
Stratix III L		✓	✓	✓				
Stratix III E		✓	✓	✓				
Stratix II			✓	✓	✓			
Stratix II GX			✓	✓	✓			
Stratix					✓	✓	✓	
Stratix GX					✓	✓	✓	

Optional Suffix

Indicates specific device options or shipment method
ES: Engineering sample
N: RoHS compliant

Ordering Codes

5SGX	E	A7	N	3	F	45	C	3	X	N	ES

Family Signature

5SE: Stratix V E
5SGS: Stratix V GS
5SGT: Stratix V GT
5SGX: Stratix V GX

Hardened IP Blocks

5SE: –
5SGS: M, E
5SGT: M
5SGX: M, E

Device Type

5SE: E9, EB
5SGS: D3, D4, D5, D6, D8
5SGT: C5, C7
5SGX: A3, A4, A5, A7, A9, AB, B5, B6

Transceiver Channels

E: 12
H: 24
K: 36
N: 48
R: 66

Transceiver Speed Grade

For Stratix V GX/GS FPGAs only
1: 14.1 Gbps
2: 12.5 Gbps
3: 8.5 Gbps

For Stratix V GT FPGAs only
2: 28.05 Gbps
3: 25.78 Gbps

Package Type

F: FineLine BGA
H: Hybrid FineLine BGA

Pin Count

Package size (mm)	Pin count
29	780
35	1,152
40	1,517
43	1,760
45	1,932

Operating Temperature

C: Commercial (0˚C to 85˚C)
I: Industrial (-40˚C to 100˚C)

Core Speed

Devices	Fast ← 1	2	3	4	5	6	7	Slow → 8
Stratix V GT		✓	✓					
Stratix V GX		✓	✓	✓				
Stratix V GS		✓	✓	✓				
Stratix V E			✓	✓				

Optional Character

TBD

Lead-Free Packaging

N: Lead-free packaging

Optional Suffix

ES: Engineering sample

Ordering Codes

5AGX	B	A7	D	4	F	27	C	4	X	N

Family Signature

5AGX: Arria V GX
5AGT: Arria V GT

Hardened IP Blocks

5AGX: B, M, F
5AGT: M, F

Device Type

5AGX: A1, A3, A5, A7, B1, B3, B5, B7
5AGT: D3, D5

Transceiver Channels

D: 9
E: 12
G: 18
H: 24
K: 36

Transceiver Speed Grade

For Arria V GX FPGAs only
4: 6.375 Gbps
6: 3.125 Gbps

For Arria V GT FPGAs only
3: 10.3125 Gbps

Package Type

F: FineLine BGA

Pin Count

Package size (mm)	Pin count
27	672
29	780
31	896
35	1,152
40	1,517

Operating Temperature

A: Automotive (-40°C to 125°C)
C: Commercial (0°C to 85°C)
I: Industrial (-40°C to 100°C)

Core Speed

Devices	Fast ← 1	2	3	4	5	6	7	8 → Slow
Arria V GX				✓	✓	✓		
Arria V GT					✓			

Optional Character

TBD

Optional Suffixes

N: Lead-free packaging
ES: Engineering sample
NES: Lead-free packaging, engineering sample

Ordering Codes

Family Signature

5ASX: Arria V SX
5AST: Arria V ST

Hardened IP Blocks

5ASX: B, M, F
5AST: F

Device Type

5ASX: B3, B5
5AST: D3, D5

Transceiver Channels

D: 9
E: 12
G: 18
H: 24
K: 30

Transceiver Speed Grade

For Arria V SX FPGAs only
4: 6.375 Gbps
6: 3.125 Gbps

For Arria V ST FPGAs only
3: 10.3125 Gbps

Package Type

F: FineLine BGA

Pin Count

Package size (mm)	Pin count
31	896
35	1,152
40	1,517

Operating Temperature

C: Commercial (0˚C to 85˚C)
I: Industrial (-40˚C to 100˚C)

Core Speed

Devices	Fast 1	2	3	4	5	6	7	Slow 8
Arria V SX				✓	✓	✓		
Arria V ST					✓			

Optional Suffixes

N: Lead-free packaging
ES: Engineering sample
NES: Lead-free packaging, engineering sample

Ordering Codes

5CGX	B	C3	B	6	F	17	C	7	X	N

Family Signature

5CE: Cyclone V E
5CGX: Cyclone V GX
5CGT: Cyclone V GT

Hardened IP Blocks

5CE: B, F
5CGX: B, F
5CGT: F

Device Type

5CE: A2, A4, A5, A7, A9
5CGX: C3, C4, C5,C7, C9
5CGT: D5, D7, D9

Transceiver Channels

B: 3
C: 6
D: 9
E: 12

Transceiver Speed Grade

For Cyclone GX FPGAs only
6: 3.125 Gbps
7: 2.5 Gbps

For Cyclone GT FPGAs only
5: 5 Gbps

Package Type

F: FineLine BGA

Pin Count

Package size (mm)	Pin count
17	256
19	324 / 484
23	484
27	672
31	896
35	1,152

Operating Temperature

A: Automotive (-40°C to 125°C)
C: Commercial (0°C to 85°C)
I: Industrial (-40°C to 100°C)

Core Speed

	Fast ⟷ Slow							
Devices	1	2	3	4	5	6	7	8
Cyclone V GT							✓	
Cyclone V GX						✓	✓	✓
Cyclone V E						✓	✓	✓

Optional Character

TBD

Optional Suffixes

N: Lead-free packaging
ES: Engineering sample
NES: Lead-free packaging, engineering sample

Ordering Codes

Family Signature

5CSE: Cyclone V SE
5CSX: Cyclone V SX
5CST: Cyclone V ST

Hardened IP Blocks

5CSE: B, M
5CSX: M, F
5CST: F

Device Type

5CSE: A2, A4, A5, A6
5CSX: C4, C5,C6
5CST: D5, D6

Transceiver Channels

C: 6
D: 9

Transceiver Speed Grade

For Cyclone SX/ST FPGAs only
5: 5 Gbps
6: 3.125 Gbps

Package Type

F: FineLine BGA
U: Ultra FineLine BGA

Pin Count

Package size (mm)	Pin count
19	484
23	672
31	896

Operating Temperature

A: Automotive (-40°C to 125°C)
C: Commercial (0°C to 85°C)
I: Industrial (-40°C to 100°C)

Core Speed

Devices	Fast ← 1	2	3	4	5	6	7	8 → Slow
Cyclone V SE						✓	✓	✓
Cyclone V SX						✓	✓	✓
Cyclone V ST						✓	✓	✓

Optional Single Core

S: Single core (available in hard IP block "B" variants only)

Optional Suffixes

N: Lead-free packaging
ES: Engineering sample
NES: Lead-free packaging, engineering sample

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Altera Corporation
101 Innovation Drive
San Jose, CA 95134
USA
www.altera.com

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 494 602 000

Altera Japan Ltd.
Shinjuku I Tower 32F
6-5-1, Nishi Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
www.altera.co.jp

Altera International Ltd.
Unit 11- 18, 9/F
Millennium City 1, Tower 1
388 Kwun Tong Road
Kwun Tong
Kowloon, Hong Kong
Telephone: (852) 2 945 7000
www.altera.com.cn

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